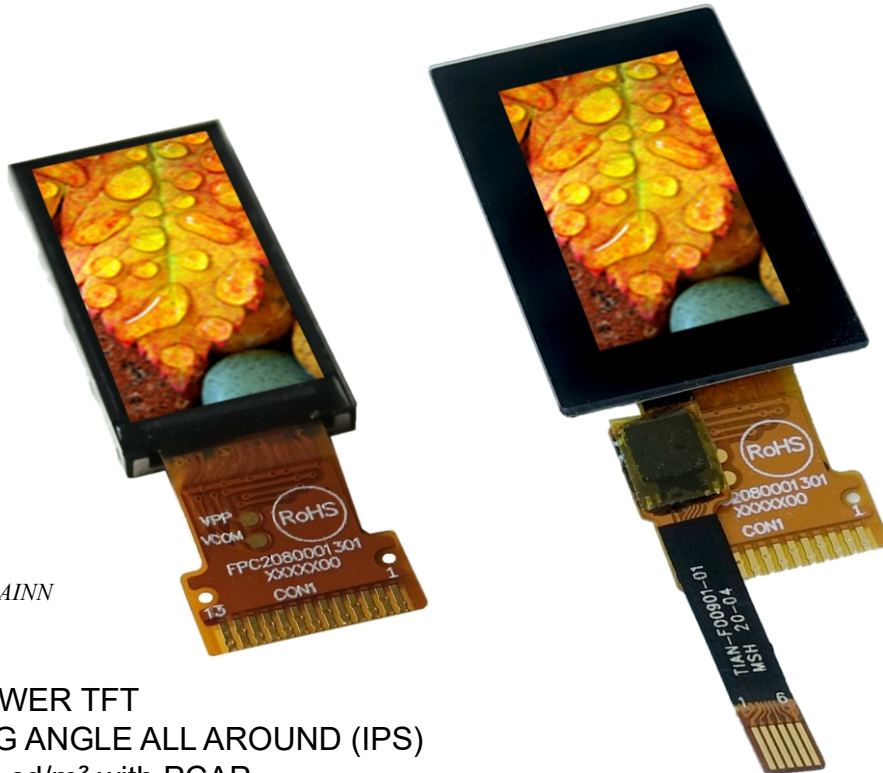


11.2025

TFT / IPS DISPLAY 160x80 DOTS 0.96"

SPI Interface incl. controller ST7735S



EA TFT009-81AINN

EA TFT009-81AITC

FEATURES

- 0.96" LOW-POWER TFT
- WIDE VIEWING ANGLE ALL AROUND (IPS)
- 500cd/m² / 400 cd/m² with PCAP
- 3.3 V SINGLE SUPPLY
- -20..+70°C (T_{OP})
- 160x80 DOTS
- INCL. CONTROLLER ST7735S
- PCAP WITH I²C BUS CONTROLLER FT3267
- 4-WIRE AND 3-WIRE SPI
- 27.95x13.5 mm OUTLINE DIMENSIONS (W. TOUCH 18.7x31.9 mm)

ORDERING CODE

- IPS 0.96" – 160X80 DOTS, INCL. ST7735S SPI
- IPS 0.96" – 160X80 DOTS, INCL. ST7735S SPI, W. PCAP (I²C)
- IPS 0.96" – 160X80 DOTS, ZIFF, INCL. ST7735S SPI
- IPS 0.96" – 160X80 DOTS, ZIFF, INCL. ST7735S SPI, W. PCAP (I²C)

- EA TFT009-81AINN
- EA TFT009-81AITC
- EA TFT009-81BINN
- EA TFT009-81BITC

- SHIELD F. RASPBERRY PICO INCL. IPS 0.96" DISPLAY
- SHIELD F. RASPBERRY PICO INCL. IPS 0.96" DISPLAY WITH PCAP

- EA RAPICOTFT009
- EA RAPICOTFT009TC

ACCESSORY

- ZIFF CONNECTOR 6-PINS 0.5mm, TOP CONTACT

- EA WF050-06S

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1. Summary

With its new 0.96" TFT display DISPLAY VISIONS launches a small-sized displays with high-quality. The IPS technology provide full viewing angle with all-angle color stability management (AACS). This means that color stays same even when viewing angle is changing. So it can be used in portrait mode 80x160 or landscape mode 160x80 direction without any disadvantage. Display brightness is typ. 500cd/m² and paves the way for manifold applications in industrially and medically field, even for usage at direct sunlight.

The displays provide 3-wire and 4-wire SPI interface which is perfect for pin saving applications. Connection is stamp soldering directly to pcb.

The version EA TFT009-81AITC comes with a PCAP touch panel. Interface for touch is I²C which makes it easy to read out directly the coordinates. Interface connection is done via 6-pin ZIF connector (not included).

There's also a version for ZIF connection available which is called EA TFT009-BINN and EA TFT009-BITC (incl. touchpanel). This one is much more simple in sample production when using a ZIF connector. Also in mass production SMT process for ZIF connection is standard and a reliable connection.

2. General Specifications

Item	Dimension	Unit
EA TFT009-81AINN/-81BINN	160x80 dots IPS display	
EA TFT009-81AITC/-81BITC	160x80 dots IPS display with PCAP touch panel	
Size	0.96	inch
Dot Matrix	80 x RGB x 160(TFT)	dots
Module dimension	13.5(W) x 27.95(H) x 1.54(D)	mm
Active area	10.8 x 21.696	mm
Dot pitch	0.135 x 0.1356	mm
LCD type	TFT, Normally black, Transmissive	
Viewing Angle	80/80/80/80	°
Aspect Ratio	1:2	
IC	ST7735S	
Interface	Display SPI Interface / PCAP I ² C bus interface	
Backlight Type	LED white	
Surface	Glare	
Touchpanel	PCAP, FT3267 or equivalent (-AITC and -BITC only)	

*Color tone slight changed by temperature and driving voltage.

3. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-20	—	+70	°C
Storage Temperature	TST	-30	—	+80	°C

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. $\leq 60^{\circ}\text{C}$, 90% RH MAX. Temp. $> 60^{\circ}\text{C}$, Absolute humidity shall be less than 90% RH at 60°C

4. Electrical Characteristics

4.1. Operating conditions:

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage TFT	VCC	3.0	3.3	3.6	V
Supply LCM current TFT	ICC	—	2	3	mA
Power supply PCAP	VDDT	2.8	—	3.3	V
	I _{VDDT}	—	4	-	mA
	I _{VDDT / Sleep}	-	50	-	μA

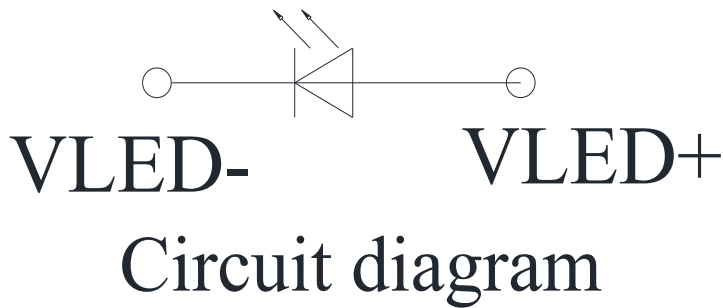
Note:

To avoid power supply noise, please avoid using driving conditions close to min. or max. value

4.2. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	I _{LED}	—	20	—	mA	
LED voltage	V _{LED}	2.8	3.0	3.3	V	Note 1
LED Life Time		—	50000	—	Hr	Note 2,3,4

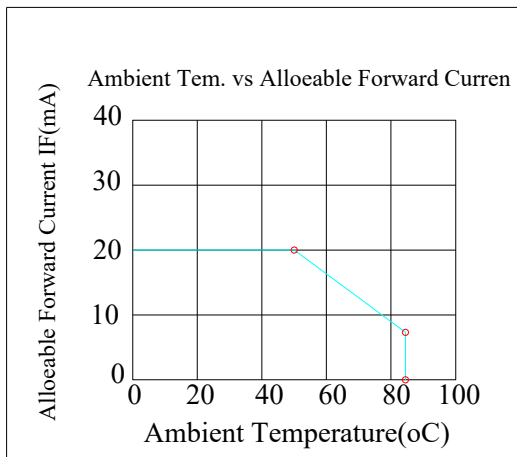
Note 1 : There is 1 LED



Note 2 : Ta = 25 °C

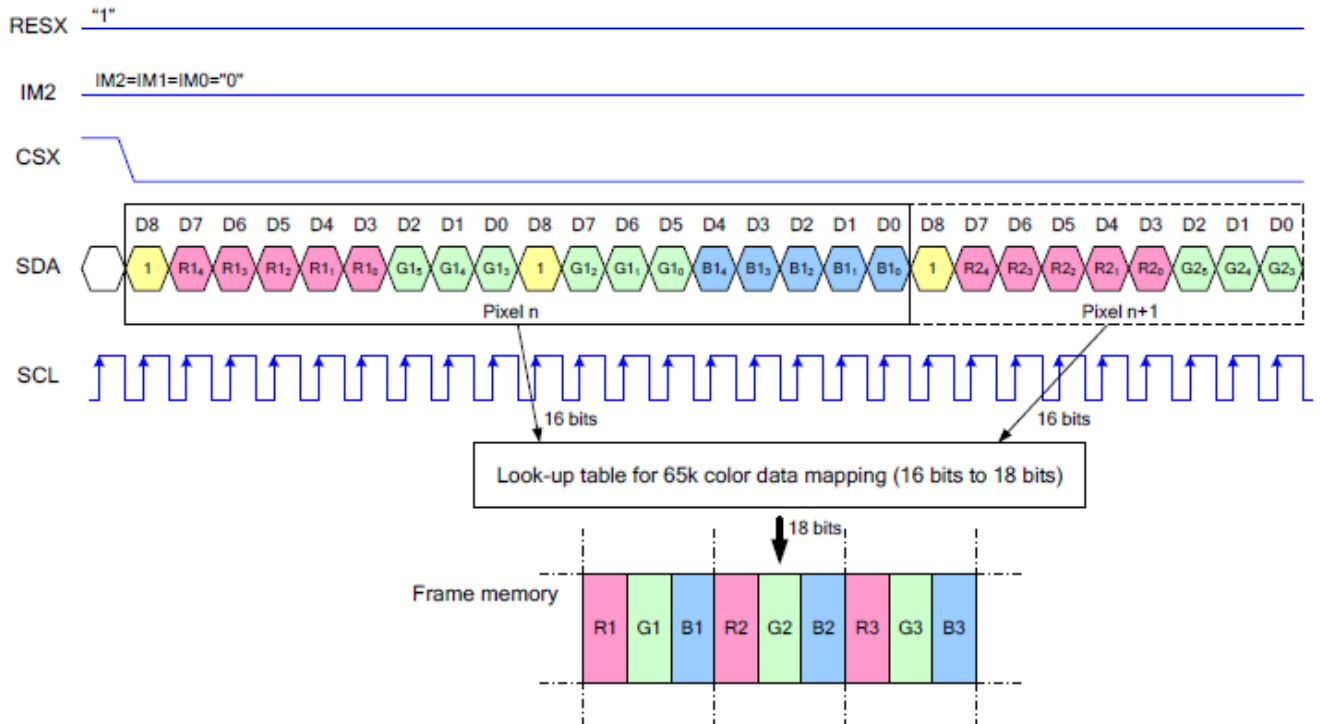
Note 3 : Brightness to be decreased to 50% of the initial value

Note 4 : The single LED lamp case



5. Data Color Coding

5.1. 3-Wire SPI Mode: RGB 5-6-5-bit Input, 65K-Colors, 3AH="05h"

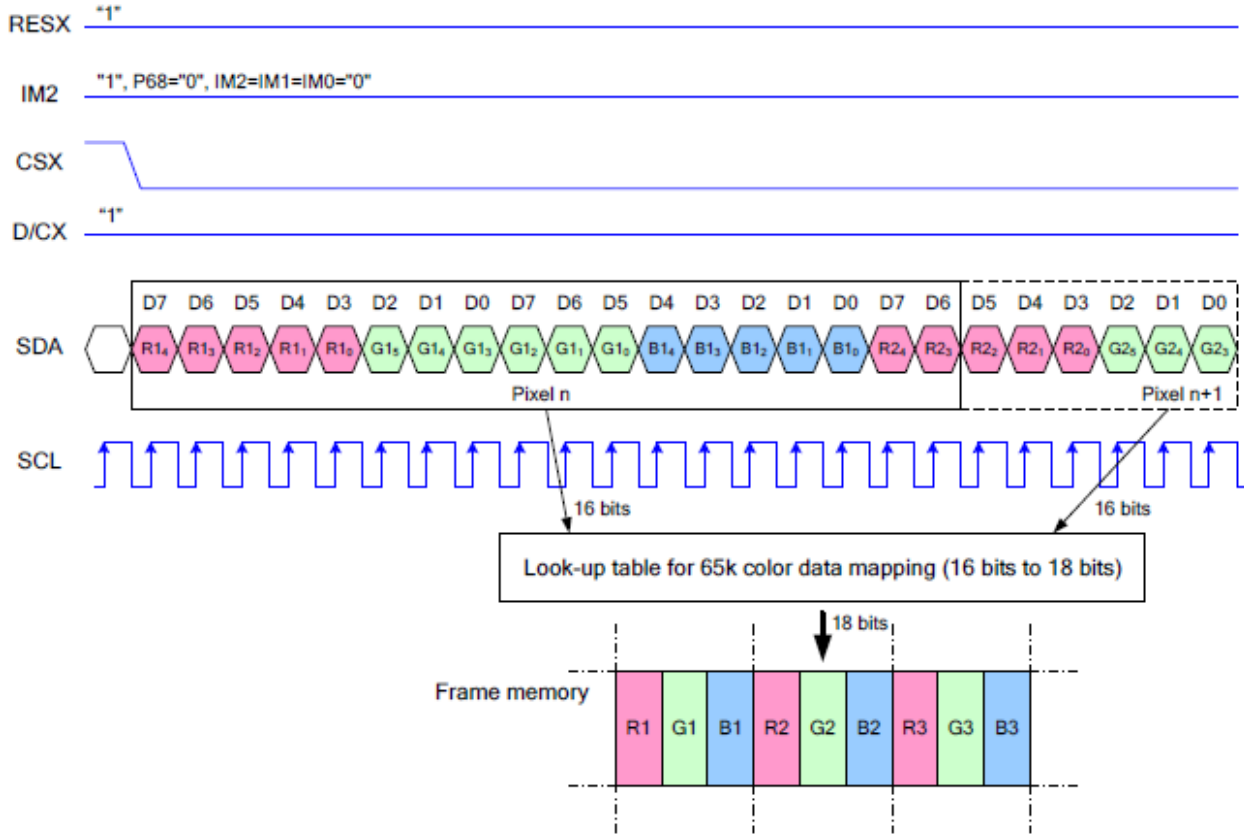


Note 1: Pixel data with the 16-bit color depth information

Note 2: The most significant bits are: Rx4, Gx5 and Bx4

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

5.2. 4-Wire SPI Mode: RGB 5-6-5-bit Input, 65K-Colors, 3AH="05h"

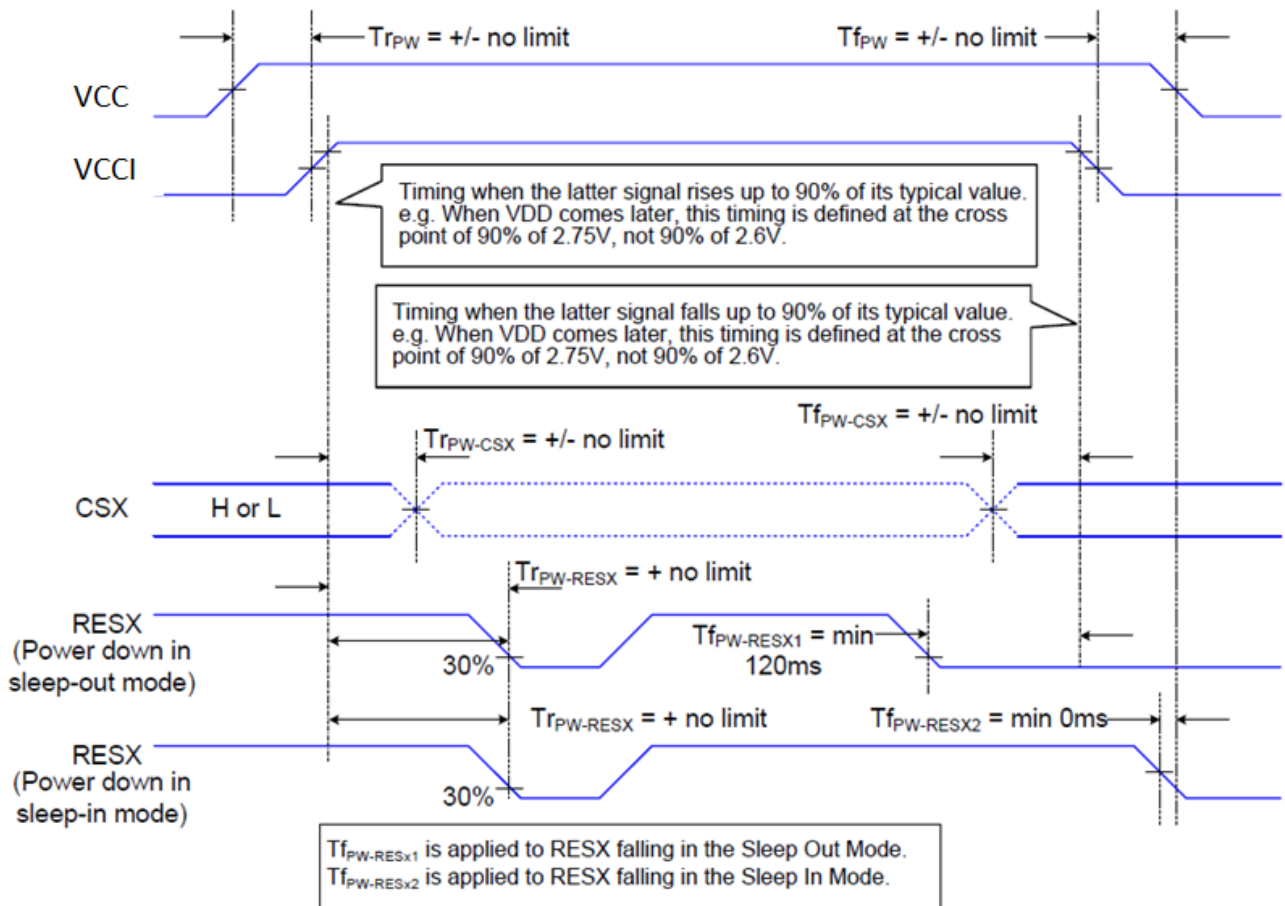


Note 1. Pixel data with the 16-bit color depth information

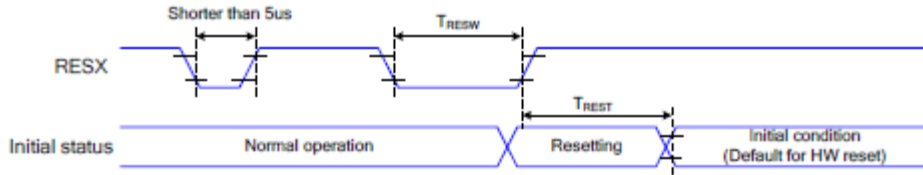
Note 2. The most significant bits are: Rx4, Gx5 and Bx4

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

6. Power ON/OFF Sequence



7. Reset Timing



Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	tRESW	Reset Pulse Duration	10	-	us
	tREST	Reset Cancel	-	5	ms
				120	ms

Table 14 Reset Timing

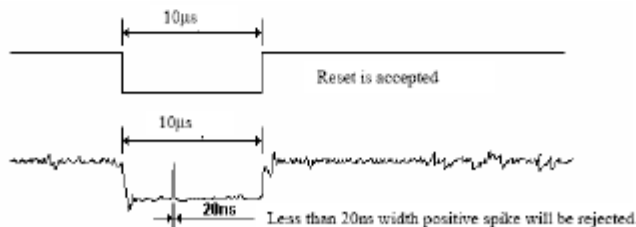
Notes:

- The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
- Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset Starts

- During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

- Spike Rejection also applies during a valid reset pulse as shown below:



- When Reset applied during Sleep In Mode.
- When Reset applied during Sleep Out Mode.
- It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Optical Characteristics

Item	Symbol	Condition.	Min	Typ.	Max.	Unit	Remark	
Response time	T_r	$\theta=0^\circ \cdot \phi=0^\circ$	-	30	40	ms	Note 3	
	T_f							
Contrast ratio	CR	At optimized viewing angle	-	800	-	-	Note 4	
Color Chromaticity	White	W_x	$\theta=0^\circ \cdot \phi=0^\circ$	0.255	0.305	0.355	Note 2,6,7	
		W_y		0.275	0.325	0.375		
Viewing angle	Hor.	Θ_R	CR \geq 10	-	80	-	Deg.	Note 1
		Θ_L		-	80	-		
	Ver.	Φ_T		-	80	-		
		Φ_B		-	80	-		
Brightness	-	AINN	400	500	-	cd/m ²	Center of display	
		AITC	300	400	-			
Uniformity	(U)	-	75	-	-	%	Note 5	

Ta=25±2°C

Note 1: Definition of viewing angle range

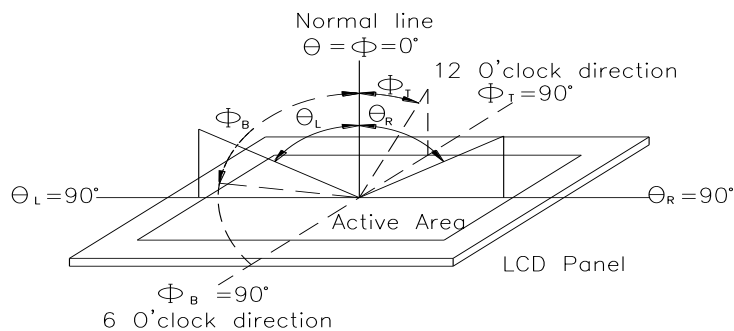


Fig.8.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7orBM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

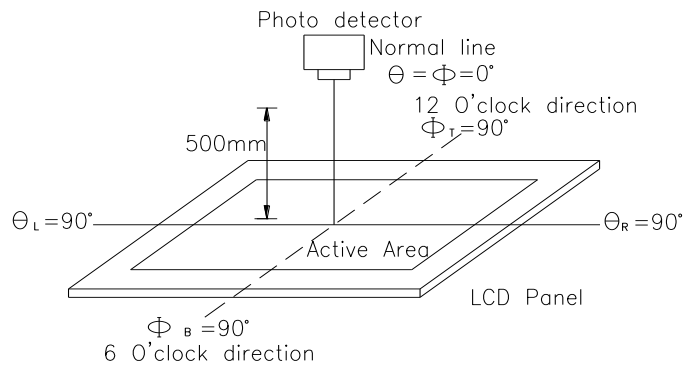
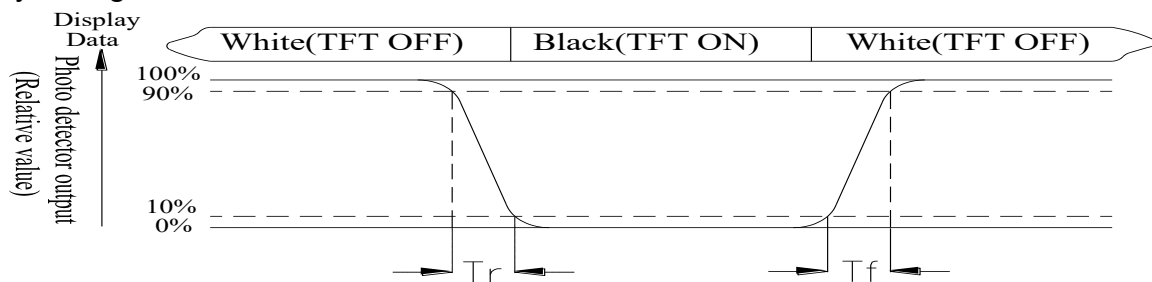


Fig. 8.2. Optical measurement system setup

Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time, T_r , is the time between photo detector output intensity changed from 90% to 10%. And fall time, T_f , is the time between photo detector output intensity changed from 10% to 90%



Note 4: Definition of contrast ratio:

The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of Luminance Uniformity

Active area is divided into 3 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity (U)} = L_{\min}/L_{\max} \times 100\%$$

L = Active area length

W = Active area width

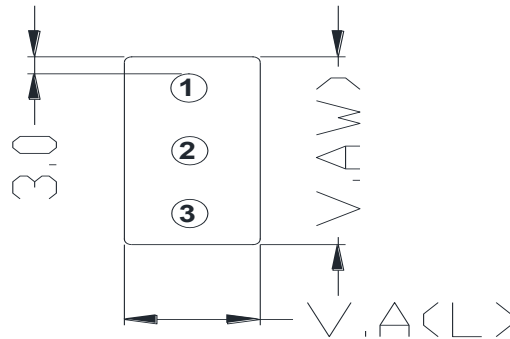


Fig9.3. Definition of uniformity

Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

9. Pinout

9.1. EA TFT009-81Axx

9.1.1 LCM PIN Definition

Pin	Symbol	Function	Remark
1	SPI4W	SPI4W='0', 3-wire SPI (9 bit) SPI4W='1', 4-wire SPI (8 bit)	
2	NC	No connection	
3	MOSI	Serial interface data (D0)	
4	CLK	Serial interface clock SCL (D/CX)	
5	WRX(D/CX)	Data/command selection pin (4-wire SPI only)	
6	RESX	Reset pin (low active)	
7	CSX	Chip selection pin (low active)	
8	GND	Ground	
9	NC	No connection	
10	VCC	Power supply	
11	LED-	Backlight cathode	
12	LED+	Backlight anode	
13	GND	Ground	

9.1.2. PCAP PIN Definition

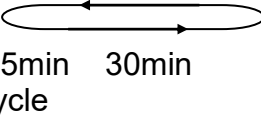
Pin	Symbol	Function	Remark
1	VDDT	Power supply	
2	SCL	I ² C clock signal. Must be pulled high	
3	SDA	I ² C data signal. Must be pulled high	
4	INT	External interrupt to the host	
5	RESET	External Reset (low active)	
6	VSS	Power ground	

9.2. EA TFT009-81Bxx for ZIFF connection

Pin	Symbol	Function	Remark
1	GND	Ground	
2	VCC	Power supply	
3	SPI4W	SPI4W='0', 3-wire SPI SPI4W='1', 4-wire SPI	
4	CLK	Serial interface clock SCL (D/CX)	
5	RESX	Reset pin (low active)	
6	CSX	Chip selection pin (low active)	
7	MOSI	Serial interface data (D0)	
8	WRX(D/CX)	Data/command selection pin (4-wire SPI only)	
9	LED-	Backlight cathode	
10	LED+	Backlight anode	
11	TP_SCL	Touchpanel I ² C clock	
12	TP_SDA	Touchpanel I ² C data	
13	TP_INT	Touchpanel interrupt	

10. Reliability

Content of Reliability Test (Wide temperature, -20°C~70°C)

Environmental Test			
Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80°C 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 200hrs	—
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max	60°C,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -20°C 25°C 70°C  30min 5min 30min 1 cycle	-20°C/70°C 10 cycles	—
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed Amplitude : 1.5mm Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z 15 minutes each	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±600V(contact), ±800v(air), RS=330Ω CS=150pF 10 times	—

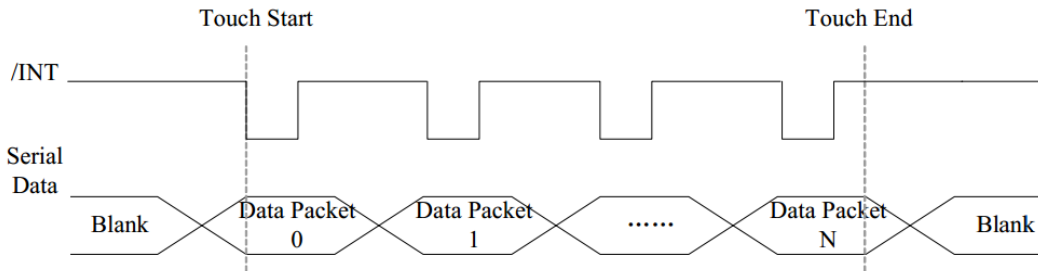
Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

Note3: The packing have to including into the vibration testing.

11. PCAP Touchpanel

Interface for PCAP is I²C bus with address 0x70. An interrupt signal to inform the host that touch data is ready for read. /INT signal will be low if there is a touch detected.

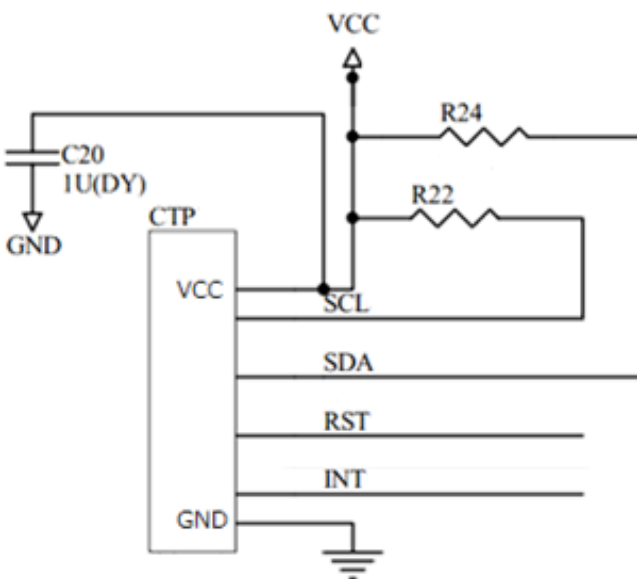


11.1 Capacitive Touch Register Description

Register No	Register Name	Bits	Value	Description
02h	Touch Points	[3:0]		The detected point number, 1
03h	Touch 1 Event Flag	[7:6]	00b	Put Down
			01b	Put Up
			10b	Contact
			11b	Reserved
03h	TOUCH1_XH	[3:0]	0h - 1h	Upper 4 bits of X touch coordinate
04h	TOUCH1_XL	[7:0]	00h - FFh	Lower 8 bits of X touch coordinate
05h	TOUCH1_YH	[3:0]	0h - 1h	Upper 4 bits of Y touch coordinate
06h	TOUCH1_YL	[7:0]	00h - FFh	Lower 8 bits of Y touch coordinate

11.2 Application Circuit

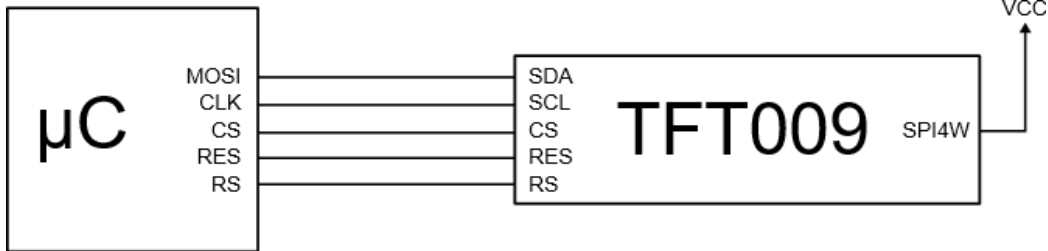
Pinout is mentioned on page 15. SCL and SDA should be pulled high externally with 7.5KΩ-10KΩ.



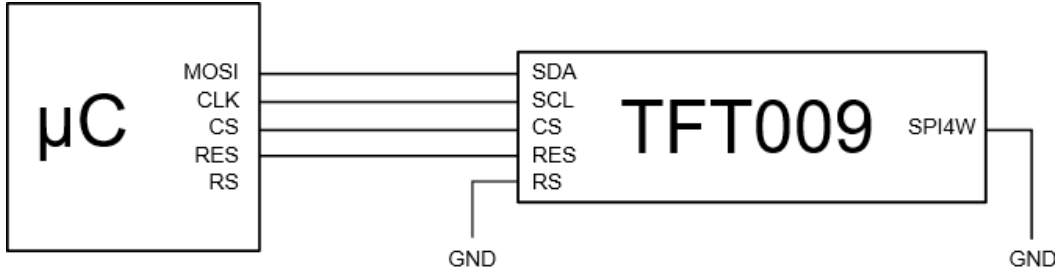
More information in data sheet FT3267 and application note.

12. Application Note Display

12.1 4-wire SPI

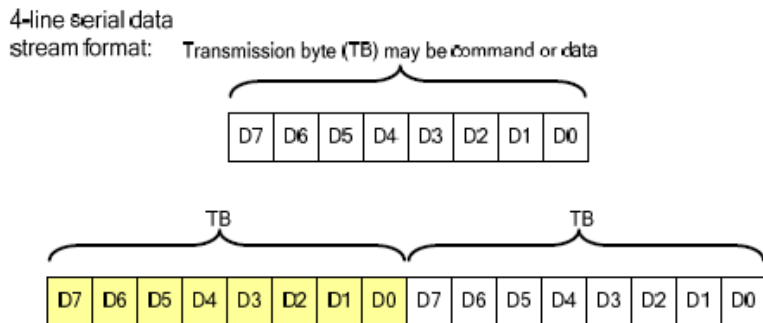
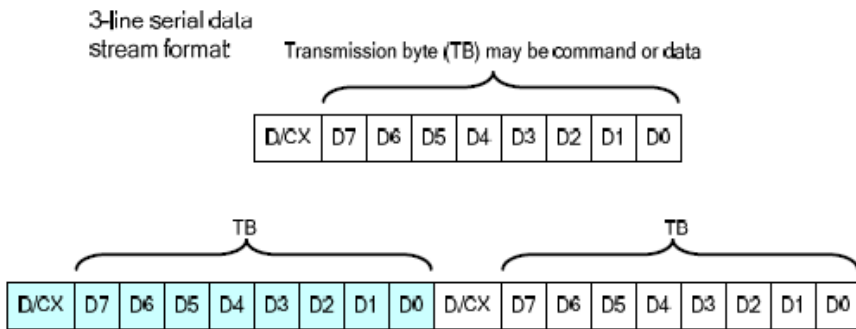


12.2 3-wire SPI



12.3 Data transfer

With 3-wire SPI there's a 9 bit data transfer, with 4-wire SPI there's a 8 bit data transfer:



13. Initial Code for Display

```
GATE = 160;
SOURCE = 80;

//RESET
SPI_RST = 1; //RA0
delay1(10);
SPI_RST = 0;
delay1(1000);
SPI_RST = 1;
delay1(10);

SPI_TFT009_WrCmd(0x11); //Sleep out
delay(120);

//ST7735S Frame Rate Setting in normal mode: fosc/
(( (RTNA*2)+40) * (LINE+FPA+BPA+2))=80
SPI_TFT009_WrCmd(0XB1); // fosc=850KHz
SPI_TFT009_WriteData(0X05); // RTNA=5
SPI_TFT009_WriteData(0X3C); //20180612 // FPA=58
SPI_TFT009_WriteData(0X3C); //20180612 // BPA=58

//ST7735S Frame Rate Setting in idle mode: fosc/ ((RTNB*2)+40) * (LINE+FPB+BPB+2))=80
SPI_TFT009_WrCmd(0XB2); // fosc=850KHz
SPI_TFT009_WriteData(0X05); // RTNB=5
SPI_TFT009_WriteData(0X3C); //20180612 // FPB=58
SPI_TFT009_WriteData(0X3C); //20180612 // BPB=58

//ST7735S Frame Rate Setting in parital mode (dot inverson): fosc/
((RTNC*2)+40) * (LINE+FPC+BPC+2))=80
//ST7735S Frame Rate Setting in parital mode (column inverson): fosc/
((RTNC*2)+40) * (LINE+FPC+BPC+2))=80
SPI_TFT009_WrCmd(0XB3); // fosc=850KHz
SPI_TFT009_WriteData(0X05); // RTNC=5
SPI_TFT009_WriteData(0X3C); //20180612 // FPC=58
SPI_TFT009_WriteData(0X3C); // BPC=58
SPI_TFT009_WriteData(0X05); // RTND=5
SPI_TFT009_WriteData(0X3C); // FPD=58
SPI_TFT009_WriteData(0X3C); // BPD=58

//ST7735S Display Inversion Control
SPI_TFT009_WrCmd(0XB4); // Dot inversion: 20184019 modify
from Sitronix initial code
SPI_TFT009_WriteData(0X07); // 0xB4[2]=Inversion setting in
normal mode // 0xB4[1]=Inversion setting in
idle mode // 0xB4[0]=Inversion setting in
partial mode
//ST7735S Power on Sequence
SPI_TFT009_WrCmd(0XC0); // power control 1
SPI_TFT009_WriteData(0XE9); //
{Par.3[0],Par.1[4:0]}=VRHP[5:0]=2→GVDD=4.6, Par.1[7:5]=AVDD [2:0]=6→AVDD=5.1
SPI_TFT009_WriteData(0X09); //
{Par.3[1],Par.2[4:0]}=VRHN[5:0]=2→GVCL=-4.6
SPI_TFT009_WriteData(0X04); // Par.3[7:6]=MODE[1:0]=2X
```

```

SPI_TFT009_WrCmd(0XC1); // power control 2
SPI_TFT009_WriteData(0XC5); // Par.1
[1:0]=VGHBT[1:0]=0→VGH=2*AVDD+VGH25-0.5

// Par.1 [3:2]=VGLSEL[1:0]=0→VGL=-7.5
[7:6]=VGLSEL[1:0]=3→VGH25=2.4

SPI_TFT009_WrCmd(0XC2); // power control 3
SPI_TFT009_WriteData(0X0D); // (Sitronix initial) {Par.1
[7:6],Par.2[7:0]=DCA[9:0]=00000000'b→Booster set up cycle BCLK/1 BCLK/3 BCLK/1
BCLK/1 BCLK/1 in normal mode
SPI_TFT009_WriteData(0X00); // Par.1[5:3]=SAPA[2:0]=001'b→ OP
current is small in normal mode // Par.1[2:0]=APA[2:0]=001'b→ OP

current is Large in normal mode
SPI_TFT009_WrCmd(0XC3); // power control 4
SPI_TFT009_WriteData(0X8D); // (Sitronix initial){Par.1
[7:6],Par.2[7:0]=DCB[9:0]=1001101010'b→Booster set up cycle BCLK/2 BCLK/1 BCLK/2
BCLK/2 BCLK/2 in idle mode
SPI_TFT009_WriteData(0X6A); // Par.1[5:3]=SAPB[2:0]=001'b→ OP
current is small in idle mode // Par.1[2:0]=APB[2:0]=011'b→ OP

current is Medium in idle mode

SPI_TFT009_WrCmd(0XC4); // power control 5
SPI_TFT009_WriteData(0X8D); // (Sitronix initial){Par.1
[7:6],Par.2[7:0]=DCC[9:0]=1011101110'b→Booster set up cycle BCLK/2 BCLK/2 BCLK/2
BCLK/4 BCLK/2 in partial mode
SPI_TFT009_WriteData(0XEE); // Par.1[5:3]=SAPC[2:0]=001'b→ OP
current is small in partial mode

// ST7735S VCOM
SPI_TFT009_WrCmd(0XC5); // VCOM setting value
SPI_TFT009_WriteData(0X15); // 0XC5[5:0]=010010'b → VCOM=-
0.875

// ST7735 Memory data access control: add from Sitronix initial code
SPI_TFT009_WrCmd(0X36); // VCOM setting value
SPI_TFT009_WriteData(0XC8); // ST7735 Display Inversion on
SPI_TFT009_WrCmd(0X21);

// ST7735 Gamma Sequence
SPI_TFT009_WrCmd(0XE0); // Gamma setting value (Positive
Polarity)
SPI_TFT009_WriteData(0X07); // Par.1[5:0]=VRF0P[5:0]=000011'b
(Variable Resistor VRHP)
SPI_TFT009_WriteData(0X0E); // Par.2[5:0]=VOS0P[5:0]=011011'b
(Variable Resistor VRLP)
SPI_TFT009_WriteData(0X08); // Par.3[5:0]=PK0P[5:0]=010010'b
(Voltage of V3 grayscale)
SPI_TFT009_WriteData(0X07); // Par.4[5:0]=PK1P[5:0]=010001'b
(Voltage of V4 grayscale)
SPI_TFT009_WriteData(0X10); // Par.5[5:0]=PK2P[5:0]=111111'b
(Voltage of V12 grayscale)
SPI_TFT009_WriteData(0X07); // Par.6[5:0]=PK3P[5:0]=111010'b

```

```

(Voltage of V20 grayscale)
SPI_TFT009_WriteData(0X02); // Par.7[5:0]=PK4P[5:0]=111010'b
(Voltage of V28 grayscale)
SPI_TFT009_WriteData(0X07); // Par.8[5:0]=PK5P[5:0]=110100'b
(Voltage of V36 grayscale)
SPI_TFT009_WriteData(0X09); // Par.9[5:0]=PK6P[5:0]=101111'b
(Voltage of V44 grayscale)
SPI_TFT009_WriteData(0X0F); // Par.10[5:0]=PK7P[5:0]=101011'b
(Voltage of V52 grayscale)
SPI_TFT009_WriteData(0X25); // Par.11[5:0]=PK8P[5:0]=110000'b
(Voltage of V56 grayscale)
SPI_TFT009_WriteData(0X36); // Par.12[5:0]=PK9P[5:0]=111010'b
(Voltage of V60 grayscale)
SPI_TFT009_WriteData(0X00); //
Par.13[5:0]=SELV0P[5:0]=000000'b (Voltage of V0 grayscale)
SPI_TFT009_WriteData(0X08); //
Par.14[5:0]=SELV1P[5:0]=000001'b (Voltage of V1 grayscale)
SPI_TFT009_WriteData(0X04); //
Par.15[5:0]=SELV62P[5:0]=000010'b (Voltage of V62 grayscale)
SPI_TFT009_WriteData(0X10); //
Par.16[5:0]=SELV63P[5:0]=001001'b (Voltage of V63 grayscale)

SPI_TFT009_WrCmd(0XE1); // Gamma setting value (Negative
Polarity)
SPI_TFT009_WriteData(0X0A); // Par.1[5:0]=VRF0N[5:0]=000011'b
(Variable Resistor VRHN)
SPI_TFT009_WriteData(0X0D); // Par.2[5:0]=VOS0N[5:0]=011011'b
(Variable Resistor VRLN)
SPI_TFT009_WriteData(0X08); // Par.3[5:0]=PK0N[5:0]=010010'b
(Voltage of V3 grayscale)
SPI_TFT009_WriteData(0X07); // Par.4[5:0]=PK1N[5:0]=010001'b
(Voltage of V4 grayscale)
SPI_TFT009_WriteData(0X0F); // Par.5[5:0]=PK2N[5:0]=110010'b
(Voltage of V12 grayscale)
SPI_TFT009_WriteData(0X07); // Par.6[5:0]=PK3N[5:0]=101111'b
(Voltage of V20 grayscale)
SPI_TFT009_WriteData(0X02); // Par.7[5:0]=PK4N[5:0]=101010'b
(Voltage of V28 grayscale)
SPI_TFT009_WriteData(0X07); // Par.8[5:0]=PK5N[5:0]=101111'b
(Voltage of V36 grayscale)
SPI_TFT009_WriteData(0X09); // Par.9[5:0]=PK6N[5:0]=101110'b
(Voltage of V44 grayscale)
SPI_TFT009_WriteData(0X0F); // Par.10[5:0]=PK7N[5:0]=101100'b
(Voltage of V52 grayscale)
SPI_TFT009_WriteData(0X25); // Par.11[5:0]=PK8N[5:0]=111001'b
(Voltage of V56 grayscale)
SPI_TFT009_WriteData(0X35); // Par.12[5:0]=PK9N[5:0]=111111'b
(Voltage of V60 grayscale)
SPI_TFT009_WriteData(0X00); //
Par.13[5:0]=SELV0N[5:0]=000000'b (Voltage of V0 grayscale)
SPI_TFT009_WriteData(0X09); //
Par.14[5:0]=SELV1N[5:0]=000000'b (Voltage of V1 grayscale)
SPI_TFT009_WriteData(0X04); //
Par.15[5:0]=SELV62N[5:0]=000001'b (Voltage of V62 grayscale)
SPI_TFT009_WriteData(0X10); //
Par.16[5:0]=SELV63N[5:0]=001001'b (Voltage of V63 grayscale)

```

```
SPI_TFT009_WrCmd(0XFC); // Enable Gate power save mode
SPI_TFT009_WriteData(0XC0); //
0XFC[7:6]=GCV_Enable[1:0]=10'b→ Gate Pump Clock Frequency disable
//
0XFC[3:2]=CLK_Variable[1:0]=11'b→ Save Power Ability is Large
SPI_TFT009_WrCmd(0X3A);
SPI_TFT009_WriteData(0X05); // 65K Mode

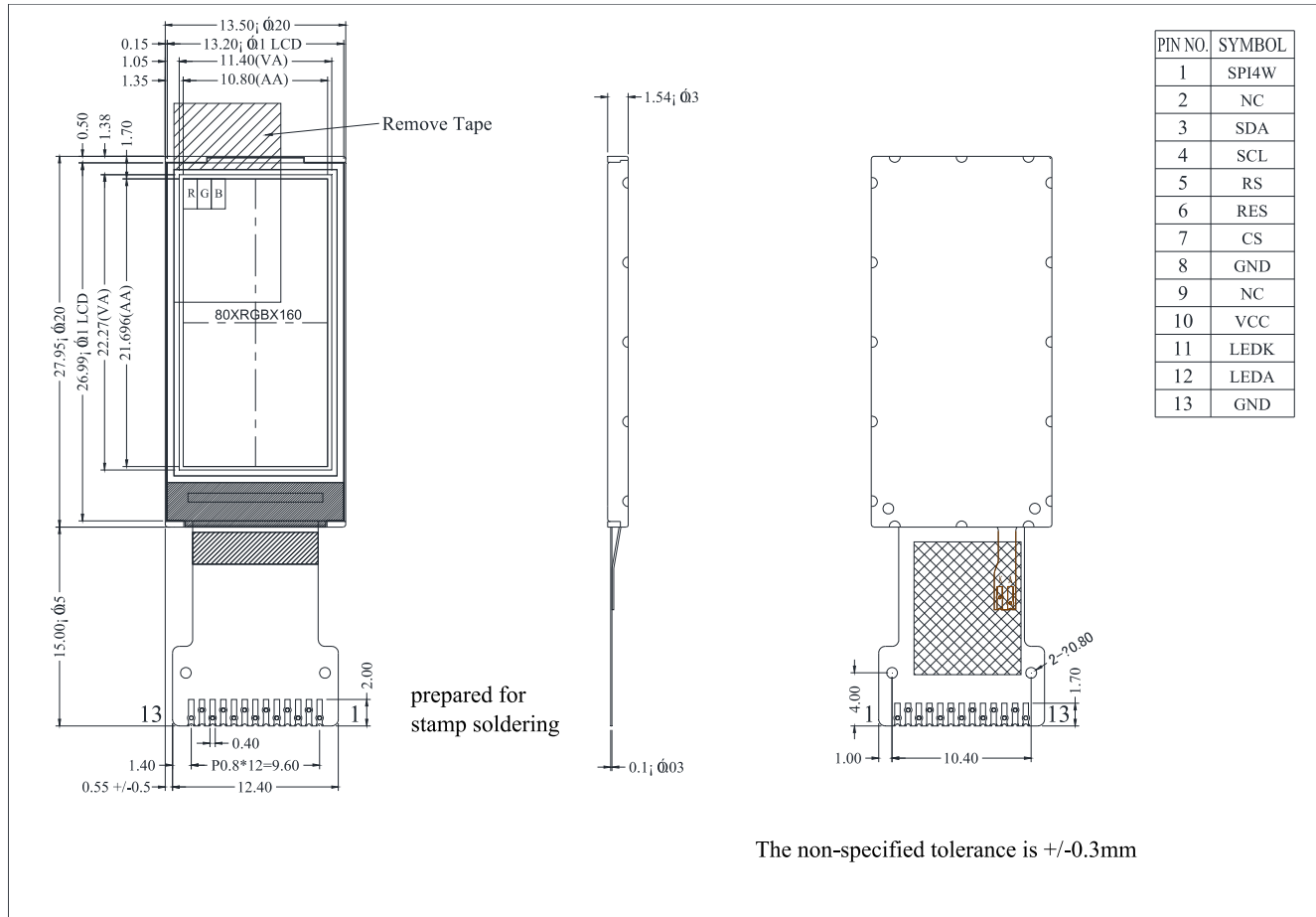
SPI_TFT009_WrCmd(0X2A);
SPI_TFT009_WriteData(0X00); // 65K Mode
SPI_TFT009_WriteData(0X1A); // 65K Mode
SPI_TFT009_WriteData(0X00); // 65K Mode
SPI_TFT009_WriteData(0X69); // 65K Mode

SPI_TFT009_WrCmd(0X2B);
SPI_TFT009_WriteData(0X00); // 6
SPI_TFT009_WriteData(0X01); //
SPI_TFT009_WriteData(0X00); //
SPI_TFT009_WriteData(0XA0); //

SPI_TFT009_WrCmd(0X29); // Display on
```

14. Contour Drawing

EA TFT009-81AINN



EA TFT009-81BITC – for ZIFF connector incl. touchpanel

Technical Drawing Details:

- Top View Dimensions:** 18.70 TP OD, 13.50±0.20 TFT OD, 10.80 TP VA, 10.80 TFT AA, 2.60±0.5, 3.95, 21.696 TP VA, 21.696 AA, 31.90 TP OD, 27.95 TFT OD, 1.83±0.5, 3.53 (0.53), 4.30±0.5, 27.00±0.5, 4.50±0.3, 2.50±0.5, 1.3, 1.3.
- Side View Dimensions:** 2.64±0.45, 1.54, 4.1±0.20, 1.65, 2.3 MAX, 0.30±0.05, 3.50±0.3, 7.00±0.1, 13, 13, 7.50, 8.09, 13.60, 2.79, 24.00±0.5.
- Labels:** Pull Tape, Lens t=0.55, Black printing, Optical bonding, Adhesive (3M9495MP T=0.14mm), ITO FILM OD 15.40, ITO FILM OD 26.93, MASKING TAPE, Stiffener, Contact side, CTP zero point (0,0), 80XRGBX160, 3.20±0.5 Bending Area, C0.15max.

Note: FPC cable is bended to the rear side. It cannot be used straight!

Table 1: Specifications

1	Lcd Type	TFT
2	Viewing Angle	80°/80°/80°
3	Screen size	0.96" (diagonal)
4	Surface	Glare
5	Display format	80XRGBX160
6	Operating Temperature	-20°C –70°C
7	Storage Temperature	-30°C –80°C
8	Active area	10.8(H) x 21.696(V)mm
9	Pixel Pitch	0.135(H) x 0.1356(V)mm
10	Color arrangement	RGB-STRIP
11	Brightness	300 min. 400 tye. cd/m2
10	CTP IC	FT3267 or equivalent
11	CTP Resolution	80*160

Table 2: Pin Connections

PNNO	SYMBOL
1	GND
2	VDD
3	SP14W
4	CLK
5	RES
6	CS
7	MOSI
8	WRX, D/C
9	VLED-
10	VLED+
11	TP_SCL
12	TP_SCA
13	TP_INT

Table 3: Revision History

REV	Revision note
Ⓒ	Modify interface tolerance
Ⓓ	Added FPC folding and fixing schematic diagram
Ⓐ	Modify FPC design and length
REV	Revision note

Table 4: Scale and Unit

SCALE: 1/1	UNIT: mm
REV: C	PAGE: 1/1

Table 5: Approval

APPROVED	08/26/2024	MODEL	EA TFT009-81BITC
CHECKED	08/26/2024	TITLE	TFT MODULE
DRAWN	LICO 08/26/2024	DWG NO.	T-090311

Circuit Diagram: VLED+ —> [Symbol] —> VLED-

Text: The non-specified tolerance of dimension is ±0.3 mm.

14.1 Bending Radius

