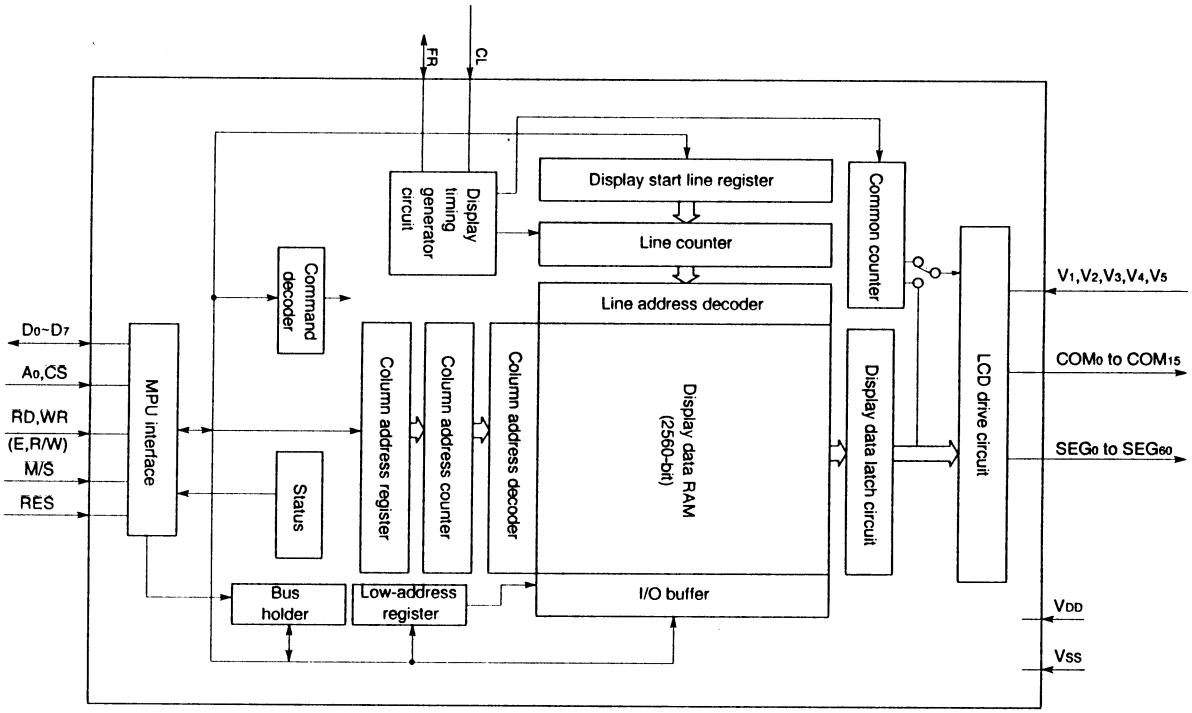
GRAPHIC CONTROLLER SED 1520



FEATURES

* FAST 8-BIT MPU INTERFACE COMPATIBLE WITH 80- AND 68-FAMILY MICROCOMPUTERS
* MANY COMMAND SET
* LOW POWER - 30µW AT 2KHZ EXTERNAL CLOCK
* WIDE RANGE OF SUPPLY VOLTAGES
* VDD - VSS: -2.4 TO -7.0 V
* VDD - VEE: -3.5 TO -13.0 V
* LOW-POWER CMOS
* INTELLIGENT ADD-ON CONTROLLER BOARD AVAILABLE (COMPLETE TEXTMODE WITH 2 CHARACTER SETS, CLEAR AREA, SET LINE ETC.): EA 9720
* COMPLETE GRAPHIC MODULES AVAILABLE: E.G. EA P122-5NLED (122x32 DOTS)

ELECTRONIC ASSEMBLY GMBH
LOCHHAMER SCHLAG 17 · D-82166 GRÄFELFING
TELEFON 089/8541991 · TELEFAX 089/8541721

PIN DESCRIPTION

(1) Power Pins

Name	Description
V_{DD}	Connected to the +5Vdc power. Common to the Vcc MPU power pin.
Vss	0 Vdc pin connected to the system ground.
V_1, V_2, V_3, V_4, V_5	Multi-level power supplies for LCD driving. The voltage determined for each liquid crystal cell is divided by resistance or it is converted in impedance by the op amp, and supplied. These voltages must satisfy the following: $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$

(2) System Bus Connection Pins

D7 to D0	Three-state I/O. The 8-bit bidirectional data buses to be connected to the 8- or 16-bit standard MPU data buses.
A0	Input. Usually connected to the low-order bit of the MPU address bus and used to identify the data or a command. A0=0: D0 to D7 are display control data. A0=1: D0 to D7 are display data.
RES	Input. When the RES signal goes ⌐└┘⌐ the 68-series MPU is initialized, and when it goes ┘┌└ , the 80-series MPU is initialized. The system is reset during edge sense of the RES signal. The interface type to the 68-series or 80-series MPU is selected by the level input as follows: High level: 68-series MPU interface Low level: 80-series MPU interface
CS	Input. Active low. Effective for an external clock operation model only. An address bus signal is usually decoded by use of chip select signal, and it is entered. If the system has a built-in oscillator, this is used as an input pin to the oscillator amp and an Rf oscillator resistor is connected to it. In such case, the RD, WR and E signals must be ORed with the CS signals and entered.
E (RD)	• <u>If the 68-series MPU is connected:</u> Input. Active high. Used as an enable clock input of the 68-series MPU. • <u>If the 80-series MPU is connected:</u> Input. Active low. The RD signal of the 80-series MPU is entered in this pin. When this signal is kept low, the SED1520 data bus is in the output status.
R/W (WR)	• <u>If the 68-series MPU is connected:</u> Input. Used as an input pin of read control signals (if R/W is high) or write control signals (if low). • <u>If the 80-series MPU is connected:</u> Input. Active low. The WR signal of the 80-series MPU is entered in this pin. A signal on the data bus is fetched at the rising edge of WR signal.

(3) LCD Drive Circuit Signals

Name	Description
CL	Input. Effective for an external clock operation model only. This is a display data latch signal to count up the line counter and common counter at each signal falling and rising edges. If the system has a built-in oscillator, this is used as an output pin of the oscillator amp and an Rf oscillator resistor is connected to it.

BLOCK DESCRIPTION

System Bus

MPU interface

1. Selecting an interface type
   The SED1520 series transfers data via 8-bit bidirectional data buses (D0 to D7). As its Reset pin has the MPU interface select function, the 80-series MPU or the 68-series MPU can directly be connected to the MPU bus by the selection of high or low $\overline{RES}$ signal level after reset (see Table 1).
   When the $\overline{CS}$ signal is high, the SED1520 series is disconnected from the MPU bus and set to stand by. However, the reset signal is entered regardless of the internal setup status.

Table 1

$\overline{RES}$ signal input level	MPU type	A0	E	R/W	CS	D0 to D7
Active low	68-series	↑	↑	↑	↑	↑
Active high	80-series	↑	$\overline{RD}$	WR	↑	↑

Data transfer

The SED1520 and SED1521 drivers use the A0, E (or $\overline{RD}$) and R/$\overline{W}$ (or $\overline{WR}$) signals to transfer data between the system MPU and internal registers. The combinations used are given in the table blow.
In order to match the timing requirements of the MPU with those of the display data RAM and control registers all data is latched into and out of the driver. This introduces a one cycle delay between a read request for data and the data arriving. For example when the MPU executes a read cycle to access display RAM the current contents of the latch are placed on the system data bus while the desired contents of the display RAM are moved into the latch.
This means that a dummy read cycle has to be executed at the start of every series of reads. See Figure 1.
No dummy cycle is required at the start of a series of writes as data is transferred automatically from the input latch to its destination.

Common	68 MPU	80 MPU		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read display data
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

Reset Circuit

Detects a rising or falling edge of an $\overline{RES}$ input and initializes the MPU during power-on.

- Initialization status
  1. Display is off.
  2. Display start line register is set to line 1.
  3. Static drive is turned off.
  4. Column address counter is set to address 0.
  5. Page address register is set to page 3.
  6. 1/32 duty (SED1520) or 1/16 duty (SED1522) is selected.
  7. Forward ADC is selected (ADC command D0 is 1 and ADC status flag is 1).
  8. Read-modify-write is turned off.

The input signal level at $\overline{RES}$ pin is sensed, and an MPU interface mode is selected as shown on Table 1. For the 80-series MPU, the $\overline{RES}$ input is passed through the inverter and the active high reset signal must be entered. For the 68-series MPU, the active low reset signal must be entered.
As shown for the MPU interface (reference example), the $\overline{RES}$ pin must be connected to the Reset pin and reset at the same time as the MPU initialization.
If the MPU is not initialized by the use of $\overline{RES}$ pin during power-on, an unrecoverable MPU failure may occur.
When the Reset command is issued, initialization items 2 and 5 above are executed.

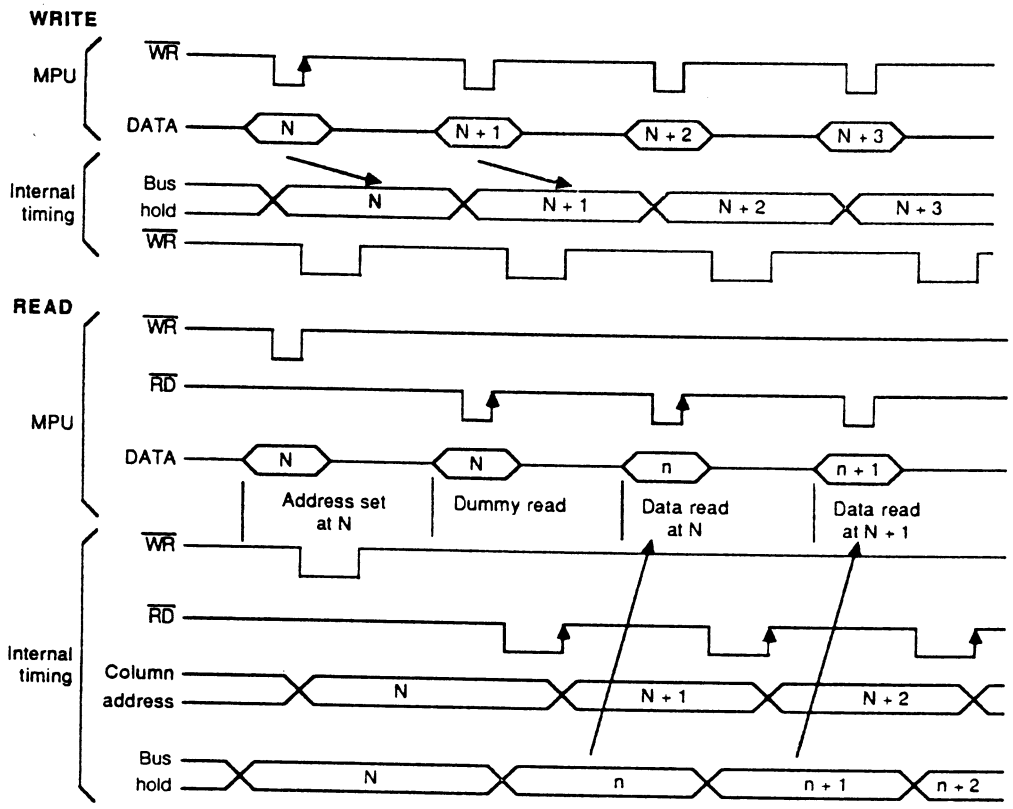


Figure 1 Bus Buffer Delay

Busy flag

When the Busy flag is logical 1, the SED1520 series is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (tcyc) is given, this flag needs not be checked at the beginning of each command and, therefore, the MPU processing capacity can greatly be enhanced.

Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command. See section 3.
The contents of the display start line register are copied into the line count register at the start of every frame, that is on each edge of FR. The line count register is incremented by the CL clock once for every display line, thus generating a pointer to the current line of data, in display data RAM, being transferred to the segment driver circuits.

Column Address Counter

The column address counter is a 7-bit presettable counter that supplies the column address for MPU access to the display data RAM. See Figure 2. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

Page Register

The page resiter is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 2. The contents of the page register are set by the Set Page Register command.

Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in Figure 2.

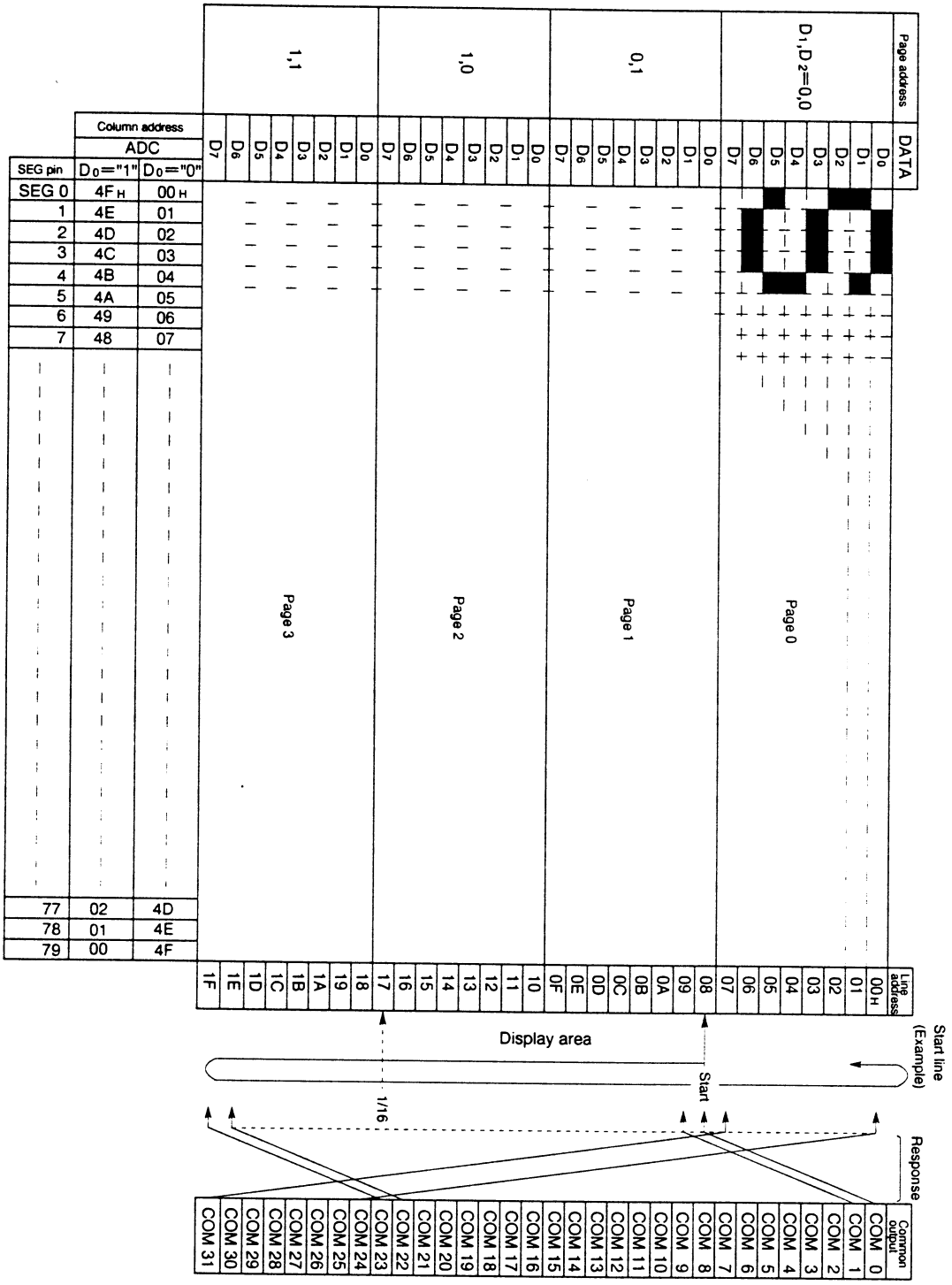


Figure 2 Display Data RAM Addressing

COMMANDS

Summary

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Display On/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1: ON, 0: OFF
Display start line	0	1	0	1	1	0	Display start address (0 to 31)					Specifies RAM line corresponding to top line of display.
Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
Set column (segment) address	0	1	0	0	Column address (0 to 79)							Sets display RAM column address in column address register.
Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status: BUSY 1: Busy 0: Ready ADC 1: CW output 0: CCW output ON/OFF 1: Display off 0: Display on RESET 1: Being reset 0: Normal
Write display data	1	1	0	Write data								Writes data from data bus into display RAM.
Read display data	1	0	1	Read data								Reads data from display RAM onto data bus.
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0: CW output, 1: CCW output
Statis drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1: Static drive, 0: Normal driving
Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selets LCD duty cycle 1: 1/32, 0: 1/16
Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON
End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF
Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset

Command Description

Table 3 is the command table. The SED1520 series identifies a data bus using a combination of A0 and R/W ($\overline{RD}$ or $\overline{WR}$) signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

Display ON/OFF

A0	$\overline{RD}$	R/W $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	1	1	D	AEH, AFH

This command turns the display on and off.

- D=1: Display ON
- D=0: Display OFF

Display Start Line

This command specifies the line address shown in Figure 3 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A0	$\overline{RD}$	R/W $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	0	A4	A3	A2	A1	A0	C0H to DFH

This command loads the display start line register.

A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	1	1	1	1	31

See Figure 2.

Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A0	$\overline{RD}$	R/W $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	1	1	0	A1	A0	B8H to BBH

This command loads the page address register.

A1	A0	Page
0	0	0
0	1	1
1	0	2
1	1	3

See Figure 2.

Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A0	$\overline{RD}$	R/$\overline{W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	A6	A5	A4	A3	A2	A1	A0	00H to 4FH

This command loads the column address register.

A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			⋮				⋮
1	0	0	1	1	1	1	79

Read Status

A0	RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

- The busy bit indicates whether the driver will accept a command or not.
  Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.
  Busy=0: The driver will accept a new command.
- The ADC bit indicates the way column addresses are assigned to segment drivers.
  ADC=1: Normal. Column address n → segment driver n.
  ADC=0: Inverted. Column address 79-u → segment driver u.
- The ON/OFF bit indicates the current status of the display.
  It is the inverse of the polarity of the display ON/OFF command.
  ON/OFF=1: Display OFF
  ON/OFF=0: Display ON
- The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.
  RESET=1: Currently executing reset command.
  RESET=0: Normal operation

Write Display Data

A0	RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

Read Display Data

A0	RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

Reads 8-bits of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.
After loading a new address into the column address register one dummy read is required before valid data is obtained.

Select ADC

A0	RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	0	0	D	A0H, A1H

This command selects the relationship between display data RAM column addresses and segment drivers.
D=1: SEG0 ← column address 4FH, ... (inverted)
D=0: SEG0 ← column address 00H, ... (normal)
This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 2 for a table of segments and column addresses for the two values of D.

Static Drive ON/OFF

A0	RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	1	0	D	A4H, A5H

Forces display on and all common outputs to be selected.
D=1: Static drive on
D=0: Static drive off

Select Duty

A0	RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	0	0	D	A8H, A9H

This command sets the duty cycle of the LCD drive and is only valid for the SED1520F and SED1522F. It is invalid for the SED1521F which performs passive operation. The duty cycle of the SED1521F is determined by the externally generated FR signal.

	SED1520	SED1522
D=1:	1/32 duty cycle	1/16 duty cycle
D=0:	1/16 duty cycle	1/8 duty cycle

When using the SED1520F0A, SED1522F0A (having a built-in oscillator) and the SED1521F0A continuously, set the duty as follows:

		SED1521F0A
SED1520F0A	1/32	1/32
	1/16	1/16
SED1522F0A	1/16	1/32
	1/8	1/16

Read-Modify-Write

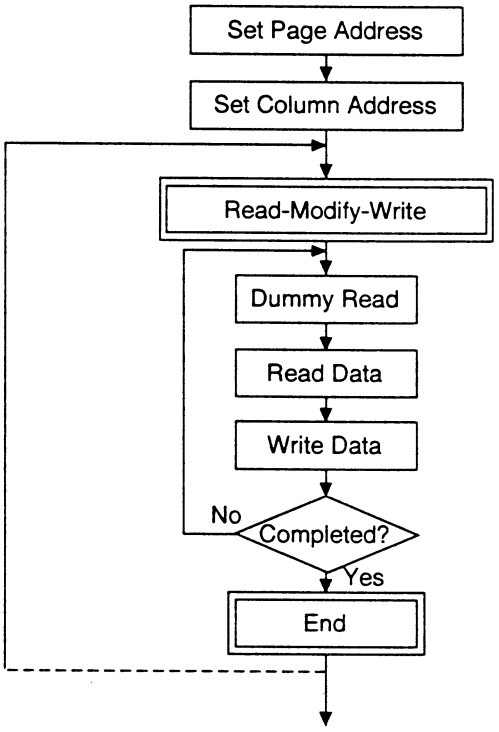
A0	$\overline{RD}$	R/$\overline{W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	0	0	E0H

This command defeats column address register auto-increment after data reads. The current conetents of the column address register are saved. This mode remains active until an End command is received.

- Operation sequence during cursor display

When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write command. This function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).

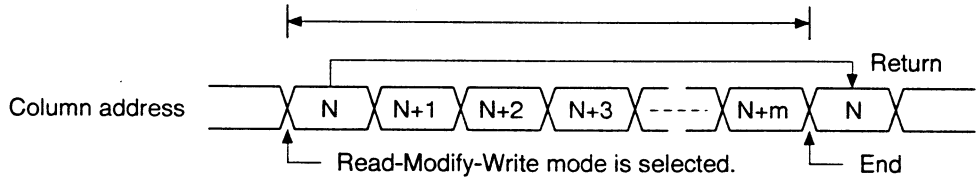
* Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.



End

A0	RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	1	1	1	0	EEH

This command cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the Read-Modify-Write command.



Reset

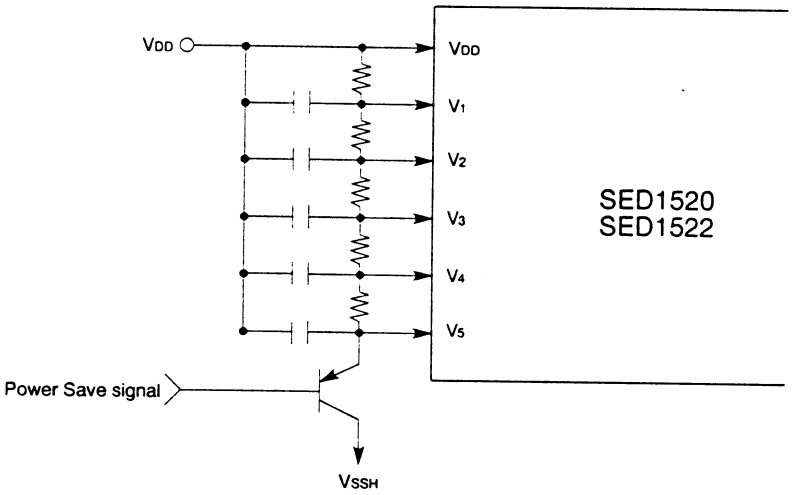
A0	RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	1	0	E2H

This command clears
- the display start line register.
- and set page address register to 3 page.
  It does not affect the contents of the display data RAM.

When the power supply is turned on, a Reset signal is entered in the $\overline{RES}$ pin. The Reset command cannot be used instead of this Reset signal.

Power Save (Combination command)

The Power Save mode is selected if the static drive is turned ON when the display is OFF. The current consumption can be reduced to almost the static current level. In the Power Save mode:
(a) The LCD drive is stopped, and the segment and common driver outputs are set to the VDD level.
(b) The external oscillation clock input is inhibited, and the OSC2 is set to the floating mode.
(c) The display and operation modes are kept.
The Power Save mode is released when the display is turned ON or when the static drive is turned OFF. If the LCD drive voltage is supplied from an external resistance divider circuit, the current passing through this resistor must be cut by the Power Save signal.



If the LCD drive power is generated by resistance division, the resistance and capacitance are determined by the LCD panel size. After the panel size has been determined, reduce the resistance to the level where the display quality is not affected and reduce the power consumption using the divider resistor.

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–8.0 to +0.3	V
Supply voltage (2)	V5	–16.5 to +0.3	V
Supply voltage (3)	V1, V4, V2, V3	V5 to +0.3	V
Input voltage	V_{IN}	Vss–0.3 to +0.3	V
Output voltage	V_O	Vss–0.3 to +0.3	V
Power dissipation	P_D	250	mW
Operating temperature	Topr	–30 to +85	deg. C
Storage temperature	Tstg	–65 to +150	deg. C
Soldering temperature time at lead	Tsol	260, 10	deg. C, sec

Notes: 1. All voltages are specified relative to V_{DD} = 0 V.
2. The following relation must be always hold
$V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

Electrical Specifications

DC Characteristics

Ta = –20 to 75 deg. C, V_{DD} = 0 V unless stated otherwise

Parameter		Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Applicable Pin
Operating voltage (1) See note 1.	Recommended	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
	Allowable				–7.0	—	–2.4		
Operating voltage (2)	Recommended	V5			–13.0	—	–3.5	V	V5 See note 10.
	Allowable				–13.0	—	—		
	Allowable	V1, V2			0.6×V5	—	V_{DD}	V	V1, V2
	Allowable	V3, V4			V5	—	0.4×V5	V	V3, V4
High-level input voltage		V_{IHT}			Vss+2.0	—	V_{DD}	V	See note 2 & 3.
		V_{IHC}			0.2×Vss	—	V_{DD}		
		V_{IHT}	Vss = –3 V		0.2×Vss	—	V_{DD}		See note 2 & 3.
		V_{IHC}	Vss = –3 V		0.2×Vss	—	V_{DD}		
Low-level input voltage		V_{ILT}			Vss		Vss+0.8		See note 2 & 3.
		V_{ILC}			Vss		0.8×Vss		
		V_{ILT}	Vss = –3 V		Vss		0.85×Vss		See note 2 & 3.
		V_{ILC}	Vss = –3 V		Vss		0.8×Vss		
High-level output voltage		V_{OHT}	I_{OH} = –3.0 mA		Vss+2.4	—	—	V	OSC2 See note 4 & 5.
		V_{OHC1}	I_{OH} = –2.0 mA		Vss+2.4	—	—		
		V_{OHC2}	I_{OH} = –120 µA		0.2×Vss	—	—		
		V_{OHT}	Vss = –3 V	I_{OH} = –2 mA	0.2×Vss			V	See note 4 & 5. OSC2
		V_{OHC1}	Vss = –3 V	I_{OH} = –2 mA	0.2×Vss				
		V_{OHC2}	Vss = –3 V	I_{OH} = –50 µA	0.2×Vss				

(continued)

DC Characteristics (Cont'd)

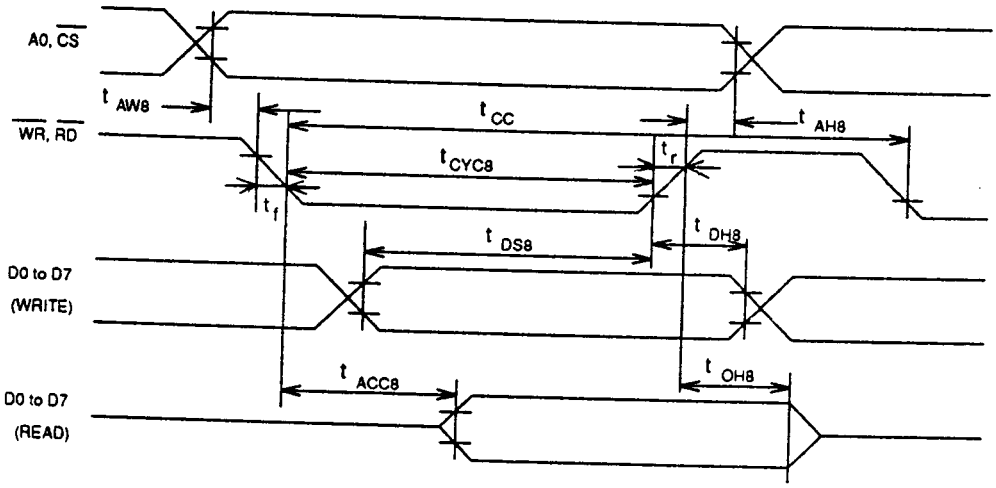
Ta = –20 to 75 deg. C, V_{DD} = 0 V unless stated otherwise

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Applicable Pin
Low-level output voltage	V_{OLT}	I_{OL} = 3.0 mA		—	—	Vss+0.4	V	OSC2 See note 4 & 5.
	V_{OLC1}	I_{OL} = 2.0 mA		—	—	Vss+0.4		
	V_{OLC2}	I_{OL} = 120 µA		—	—	0.8×Vss		
	V_{OLT}	Vss = –3 V	I_{OL} = 2 mA			0.8×Vss	V	See note 4 & 5. OSC2
	V_{OLC1}	Vss = –3 V	I_{OL} = 2 mA			0.8×Vss		
	V_{OLC2}	Vss = –3 V	I_{OL} = 50 µA			0.8×Vss		
Input leakage current	I_{LI}			–1.0	—	1.0	µA	See note 6.
Output leakage current	I_{LO}			–3.0	—	3.0	µA	See note 7.
LCD driver ON resistance	R_{ON}	Ta = 25 deg. C	V5 = –5.0 V	—	5.0	7.5	kΩ	SEG0 to 79, COM0 to 15, See note 11
			V5 = –3.5 V	—	10.0	50.0		
Static current dissipation	I_{DDQ}	CS = CL = V_{DD}		—	0.05	1.0	µA	V_{DD}
Dynamic current dissipation	I_{DD} (1)	During display V5 = –5.0 V	f_{CL} = 2 kHz	—	2.0	5.0	µA	V_{DD} See note 12, 13 & 14.
			Rf = 1 MΩ	—	9.5	15.0		
			f_{CL} = 18 kHz	—	5.0	10.0		
		During display V5 = –5 V Vss = –3 V	f_{CL} = 2 kHz		1.5	4.5	µA	V_{DD} See note 12 & 13.
			Rf = 1 MΩ		6.0	12.0		
	I_{DD} (2)	During access t_{cyc} = 200 kHz		—	300	500	µA	See note 8.
		Vss = –3V, During access t_{cyc} = 200 kHz			150	300		
Input pin capacitance	C_{IN}	Ta = 25 deg. C, f = 1 MHz		—	5.0	8.0	pF	All input pins
Oscillation frequency	f_{OSC}	Rf = 1.0 MΩ ±2%, Vss = –5.0 V		15	18	21	kHz	See note 9.
		Rf = 1.0 MΩ ±2%, Vss = –3.0 V		11	16	21		
Reset time	t_R			1.0	—		µS	RES See note 15.

Notes:
1. Operation over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.
2. A0, D0 to D7, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$) and $\overline{CS}$
3. CL, FR, M/$\overline{S}$ and $\overline{RES}$
4. D0 to D7
5. FR
6. A0, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$), $\overline{CS}$, CL, M/$\overline{S}$ and $\overline{RES}$
7. When D0 to D7 and FR are high impedance.
8. During continual write acess at a frequency of t_{cyc}. Current consumption during access is effectively proportional to the access frequency.
9. See figure below for details
10. See figure below for details
11. For a voltage differential of 0.1 V between input (V1, ..., V4) and output (COM, SEG) pins. All voltages within specified operating voltage range.
12. SED1520*A* and SED1521*A* and SED1522*A* only. Does not include transient currents due to stray and panel capacitances.
13. SED1520*0* and SED1522*0* only. Does not include transient currents due to stray and panel capacitances.
14. SED1521*0* only. Does not include transient currents due to stray and panel capacitances.
15. t_R (Reset time) represents the time from the RES signal edge to the completion of reset of the internal circuit. Therefore, the SED1520 series enters the normal operation status after this t_R.

AC Characteristics

- MPU Bus Read/Write I (80-family MPU)



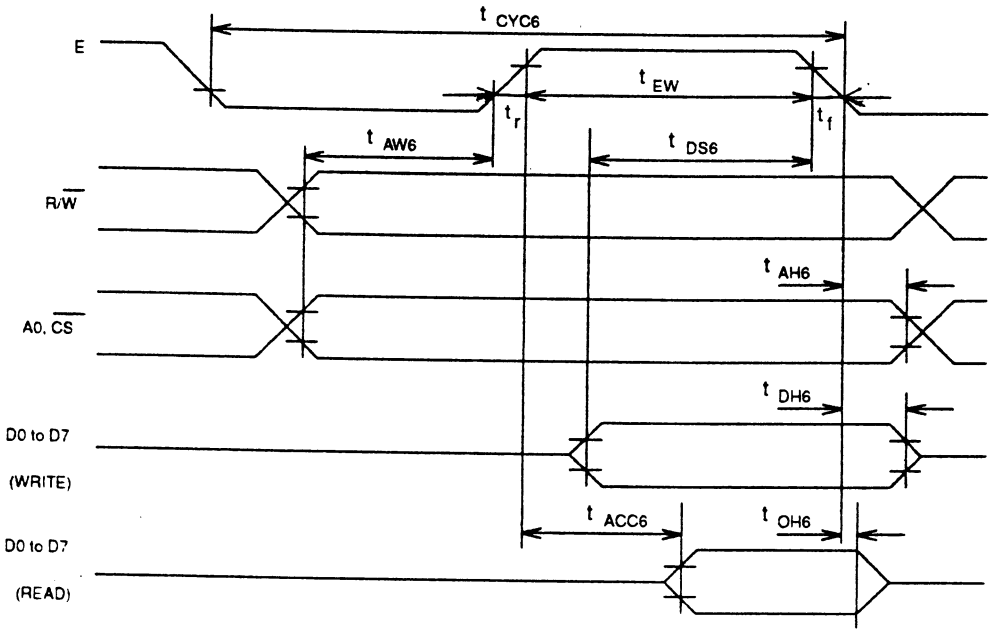
Ta = –20 to 75 deg. C, Vss = –5.0 V ±10% unless stated otherwise

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
Address hold time	tAH8		10	—	ns	A0, CS
Address setup time	tAW8		20	—	ns	
System cycle time	tCYC8		1000	—	ns	WR, RD
Control pulsewidth	tCC		200	—	ns	
Data setup time	tDS8		80	—	ns	D0 to D7
Data hold time	tDH8		10	—	ns	
RD access time	tACC8	CL = 100 pF	—	90	ns	
Output disable time	tCH8		10	60	ns	
Rise and fall time	tr, tf	—	—	15	ns	—

(Vss = –2.7 to –4.5 V, Ta = –20 to +75°C)

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
Address hold time	tAH8	—	20	—	ns	A0, CS
Address setup time	tAW8		40	—	ns	
System cycle time	tCYC8	—	2000	—	ns	WR, RD
Control pulse width	tCC		400	—	ns	
Data setup time	tDS8	—	160	—	ns	D0 to D7
Data hold time	tDH8		20	—	ns	
RD access time	tACC8	CL = 100 pF	—	180	ns	
Output disable time	tCH8		20	120	ns	
Rise and fall time	tr, tf	—	—	15	ns	—

- MPU Bus Read/Write II (68-family MPU)



Ta = –20 to 75 deg. C, Vss = –5 V ±10 unless stated otherwise

Parameter		Symbol	Condition	Rating		Unit	Signal
				Min.	Max.		
System cycle time		tCYC6		1000	—	ns	A0, CS, R/W
Address setup time		tAW6		20	—	ns	
Address hold time		tAH6		10	—	ns	
Data setup time		tDS6		80	—	ns	D0 to D7
Data hold time		tDH6		10	—	ns	
Output disable time		tOH6	CL = 100 pF	10	60	ns	
Access time		tACC6		—	90	ns	
Enable pulsewidth	Read	tEW		100	—	ns	E
	Write			80	—	ns	
Rise and fall time		tr, tf	—	—	15	ns	—

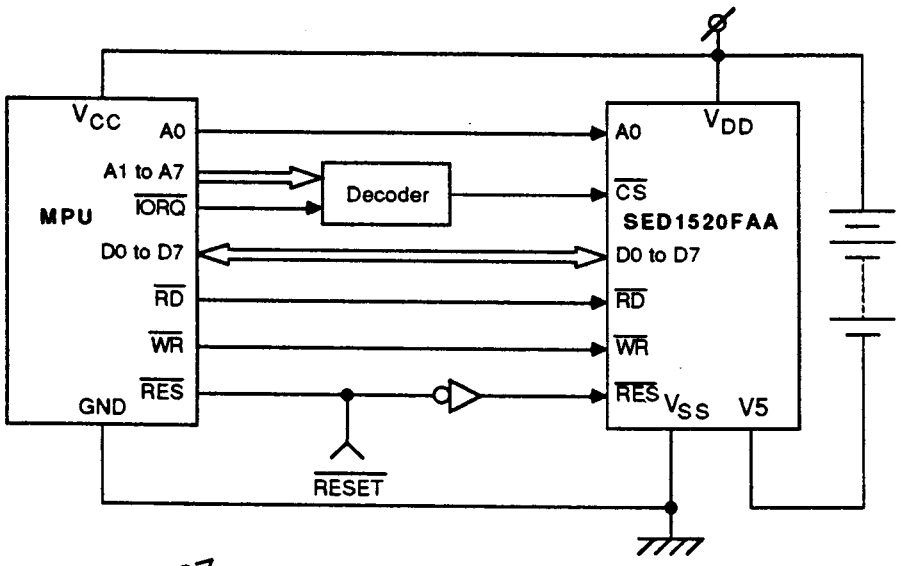
(Vss = –2.7 to – 4.5 V, Ta = –20 to +75°C)

Parameter		Symbol	Condition	Rating		Unit	Signal
				Min.	Max.		
System cycle time[1]		tCYC6	—	2000	—	ns	A0, CS, R/W
Address setup time		tAW6	—	40	—	ns	
Address hold time		tAH6		20	—	ns	
Data setup time		tDS6	—	160	—	ns	D0 to D7
Data hold time		tDH6		20	—	ns	
Output disable time		tOH6	CL = 100 pF	20	120	ns	
Access time		tACC6		—	180	ns	
Enable pulse width	Read	tEW	—	200	—	ns	E
	Write			160	—	ns	
Rise and fall time		tr, tf	—	—	15	ns	—

Notes: 1. tCYC6 is the cycle time of $\overline{CS}$. E = H, not the cycle time of E.

USER MANUAL SED 1520

APPLICATION NOTES
MPU Interface Configuration
80 Family MPU



lieferbar Ende Juni '97

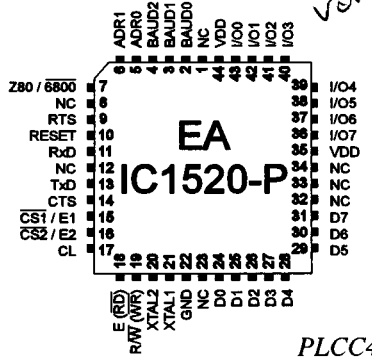
HIGH-LEVEL Grafikkontroller für Displays mit SED 1520

3.97

TECHNISCHE DATEN

* FÜR LC GRAFIKDISPLAYS 122x32 (120x32) MIT SED 1520
* KEINE TIMINGPROBLEME MEHR BEI SCHNELLEM BUSSYSTEM
* PROGRAMMIERUNG ÜBER HOCHSPRACHENÄHNLICHE BEFEHLE:
* GERADE, PUNKT, BEREICH, UND/ODER/EXOR, BARGRAPH...
* 3 VERSCHIEDENE FONTS INTEGRIERT
* ZOOM FUNKTION (2-, 3- UND 4-FACH) ALLER FONTS
* 4-16 FREI DEFINIERBARE ZEICHEN (JE NACH GRÖßE)
* TEXT UND GRAFIK MISCHEN
* ANSTEUERUNG ÜBER RS-232 / CMOS-PEGEL
* DIREKTER ANSCHLUß VON ICL232 O.Ä. MÖGLICH
* BAUDRATE PROGRAMMIERBAR VON 150 BIS 115.200 BAUD
* BELASTET NICHT DAS PROZESSORSYSTEM
* NUR 4 EXTERNE BAUTEILE ERFORDERLICH
* 8 DIGITALE I/O´S ZUR FREIEN VERWENDUNG
* HARDWARE CODIERUNG VON BIS ZU 4 ADRESSEN

vorläufig
Techn. Änderungen vorbehalten



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BESTELLBEZEICHNUNG

HIGH-LEVEL GRAFIKKONTROLLER 122x32 FÜR SED1520	**EA IC1520-PGH**
KERAMIKRESONATOR SMD 7,37MHz, 3 PINS INKL. C´s	**EA KERS7M37-C**
PASSENDES GRAFIKDISPLAY MIT SED1520, 122x32	**EA P122-NLED**

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