Princeton Technology Corp.
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DESCRIPTIONS

PT6608 is a 64 -channel segment driver for dot matrix liquid crystal graphic display system. It utilizes CMOS Technology and provides display RAM, 64-bit data latch, 64 bit drivers and decoder logics. It features the internal display RAM used as storage for the display data which are transferred from an 8-bit microcontroller. It generates the dot matrix liquid crystal driving signals corresponding to the given stored data. Paired with PT6607 (Common Driver IC), PT6608's pin assignments and application circuit are optimized for easier PCB Layout and cost saving advantages.

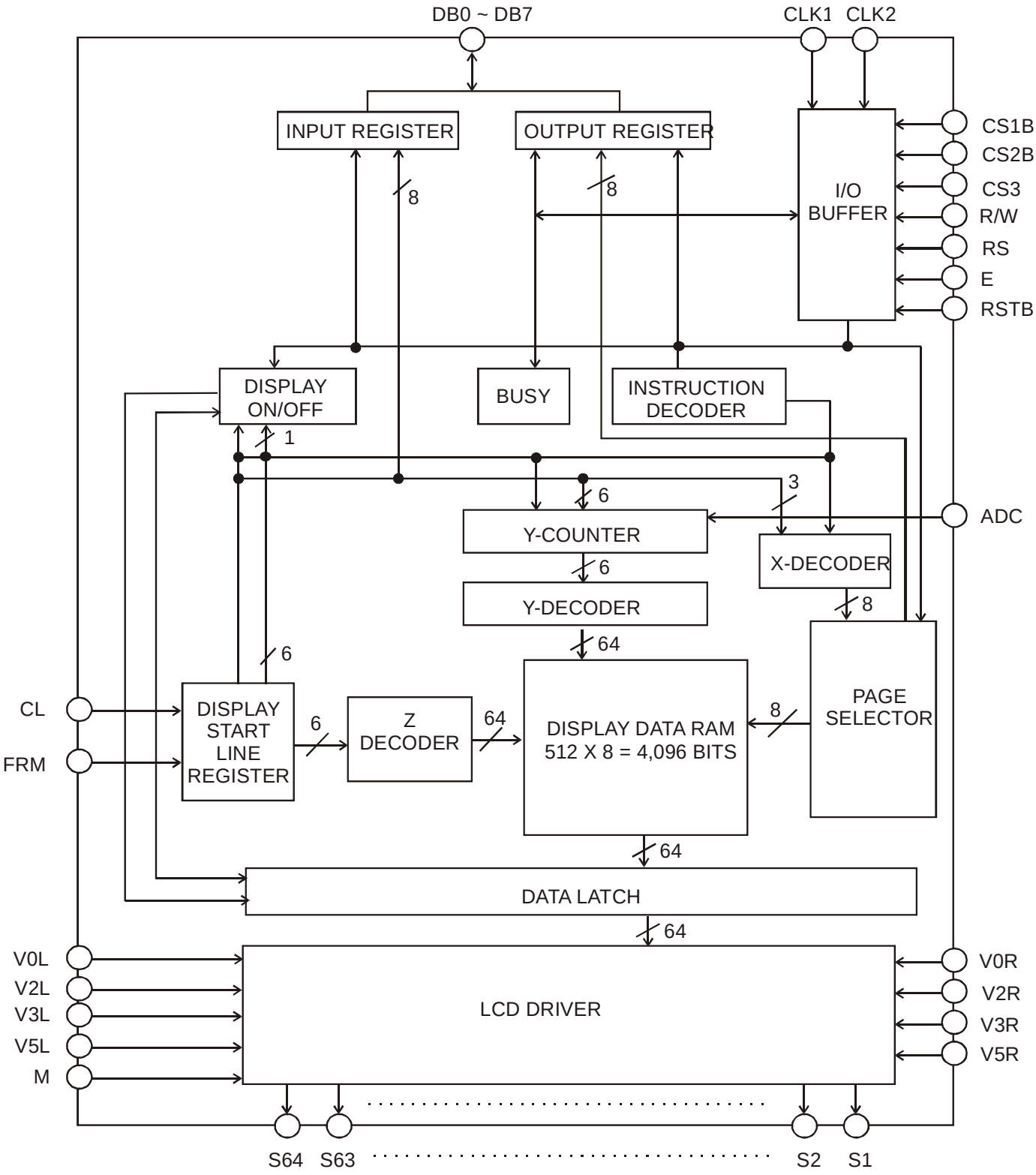
FEATURES

- CMOS Technology
- LCD Driving Voltage: 8 V to 17 V (VDD-VEE)
- Power Supply Voltage: +5V ± 10 %
- LCD Duty: 1/32 to 1/64
- Display Data is stored in Display Data RAM from MPU
- Provides 64-Channel Output
- Available in C.O.B. or 100-Pin, QF Package
- Output: 64 Channel for LCD Driving
- Input: 8 Bits Parallel Display Data
    - Control Signal from MPU
    - Splitted Bias Voltage (V0R, V0L, V2R, V2L, V3R, V3L, V5R, V5L)
- Interface: Common Driver - PT6607
    - Segment Driver - PT6608
    - Controller - MPU

APPLICATIONS

- Peripheral devices

BLOCK DIAGRAM



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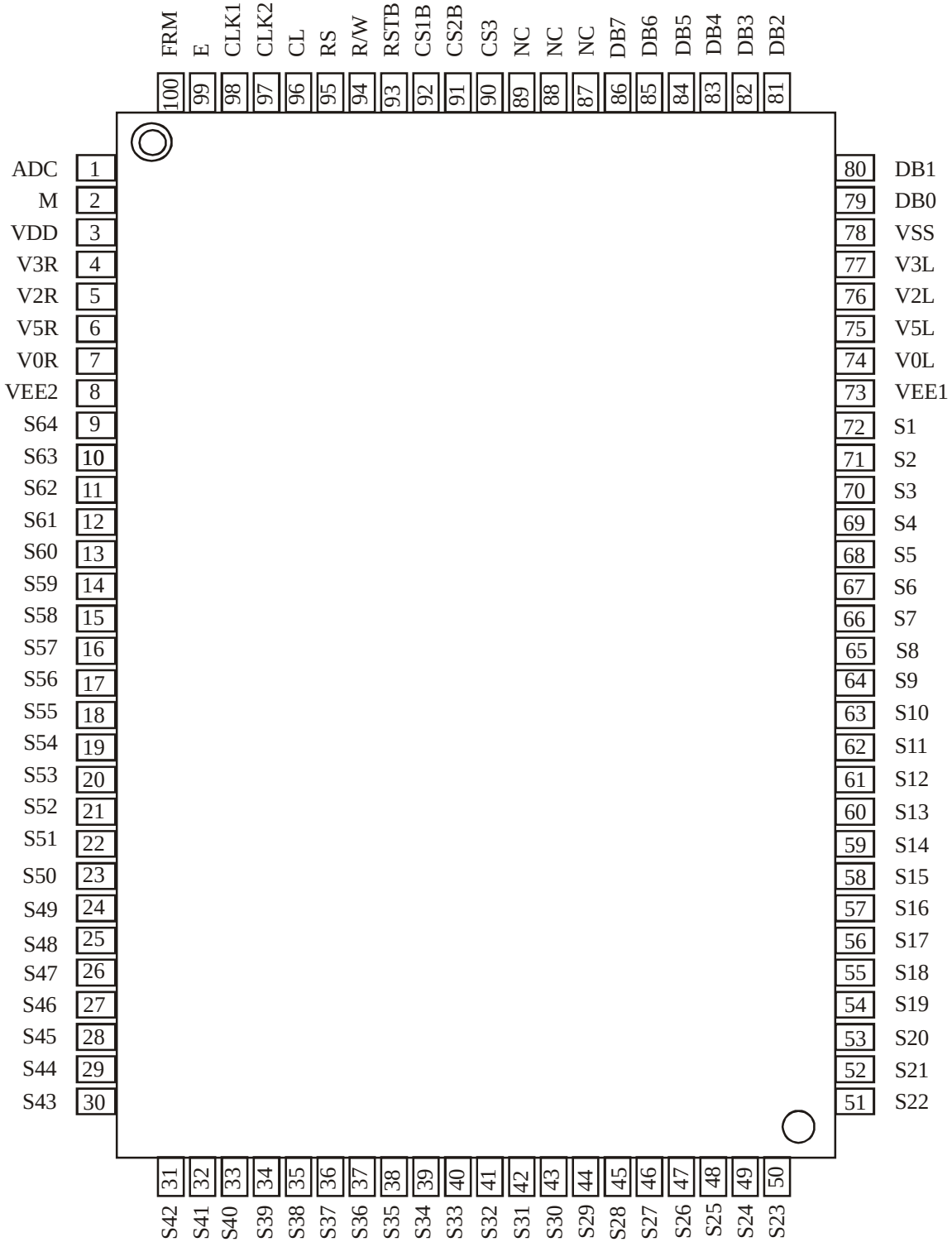
PIN CONFIGURATION



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PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
ADC	I	Address Control Signal Pin This pin determines the relationship between the Y address of the Display RAM and the terminals from which the data is outputted. ADC=High → Y0:S1 ~Y63:S64 ADC=Low → Y0:S64 ~ Y63:S1	1
M	I	Alternating Signal Input Pin for driving LCD	2
VDD	-	Internal Logic Circuit Power Supply	3
V3R,V3L V2R,V2L	-	Bias Supply Voltage Non Select Level: V2L,V2R,V3L,V3R	4,77 5,76
V5R,V5L V0R,V0L	-	Bias Supply Voltage Select Level: V0L,V0R,V5L,V5R	6,75 7,74
VEE2, VEE1	-	LCD Driver Circuit Power Supply VEE1 and VEE2 are connected to the same voltage.	8, 73
S64 to S1	O	LCD Segment Driver Output Pin	9 to 72
VSS	-	GND (0V)	78
DB0 to DB7	I/O	Data Bus Input/Output Pin	79 to 86
NC	-	No Connection	87 to 89
CS3, CS1B, CS2B	I	Chip Select Pin	90 to 92
RSTB	I	Reset Signal Input Pin When RSTB is ”LOW”: 1. ON/OFF Register is set to “0” (DISPLAY OFF) 2. Display Start Line Register is set to “0” (Z-Address 0 set, Display from line 0) After reset is released, this condition can only be changed by instruction.	93
R/W	I	R/W Input Pin When this pin is set to “H”, READ mode is active. Data is displayed at DB0 to DB7 and can be read by the CPU with E = “H”, CS1B = “L”, and CS3 = “H”. When this pin is set to “L”, WRITE mode is active. Data is displayed at DB0 to DB7 and are latched at the falling edge of E when SC1B = “L”, CS2B = “L”, and CS3 = “H”.	94
RS	I	Data/Instruction Select Input Pin RS = “H” DB0 to DB7 = display RAM dataRS = “L” DB0 to DB7 = instruction data	95
CL	I	Display Synchronous Signal Input Pin Display data is latched at the rising edge of the CL signal and increments the Z-address counter at the falling edge of the CL signal.	96

Pin Name	I/O	Description	Pin No.
CLK2, CLK1	I	Phase Clock Signal Input Pin These pins are used to execute operations for the input/output of the display RAM and other data.	97, 98
E	I	Enable Signal Input Pin	99
FRM	I	Synchronous Control Signal Input Pin This pin presets the 6-bit Z counter and synchronizes the common signal when the frame signal becomes “H”.	100

FUNCTIONAL DESCRIPTION

I/O BUFFER

The Input Buffer is used to enable or disable PT6608. CS1B to CS3 must be active in order for the input or output of data and instruction to be executed. The internal state is not changes, but RSTB and ADC can operate irrespective of CS1B to CS3.

INPUT REGISTER

Input register is used to interface with the MPU and temporarily store the data before writing to the display RAM. When CS1B to CS3 are active, the input register are selected by R/W and RS. The data from the MPU is written into the input register and then written into the display RAM. The data is latched at the falling edge of the E signal and is written automatically into the display data RAM by internal operation.

OUTPUT REGISTER

The output register is used to temporarily store the display data RAM when CS1B to CS3 are active and R/w and RS are set to High. The stored data in the display data RAM is latched in the Output Register. When CS1B to CS3 are active, R/W is set to High, and RS is set to Low -- the status data (busy check) can be read out.

You need to access the read instruction twice in order to read the contents of the display data RAM. During the first access, the data in the display data RAM is latched into the output register. During the second access, MPU reads the latched data. Thus, to read the data in the display data RAM, a dummy read is required; however, a dummy read is not needed in the status read. Please refer to the table below.

RS	R/W	Function
L	L	Instruction
L	H	Status Read (Busy Check)
H	L	Data Write (from Input Register to Display Data RAM)
H	H	Data Read (from Display Data RAM to Output Register)

RESET

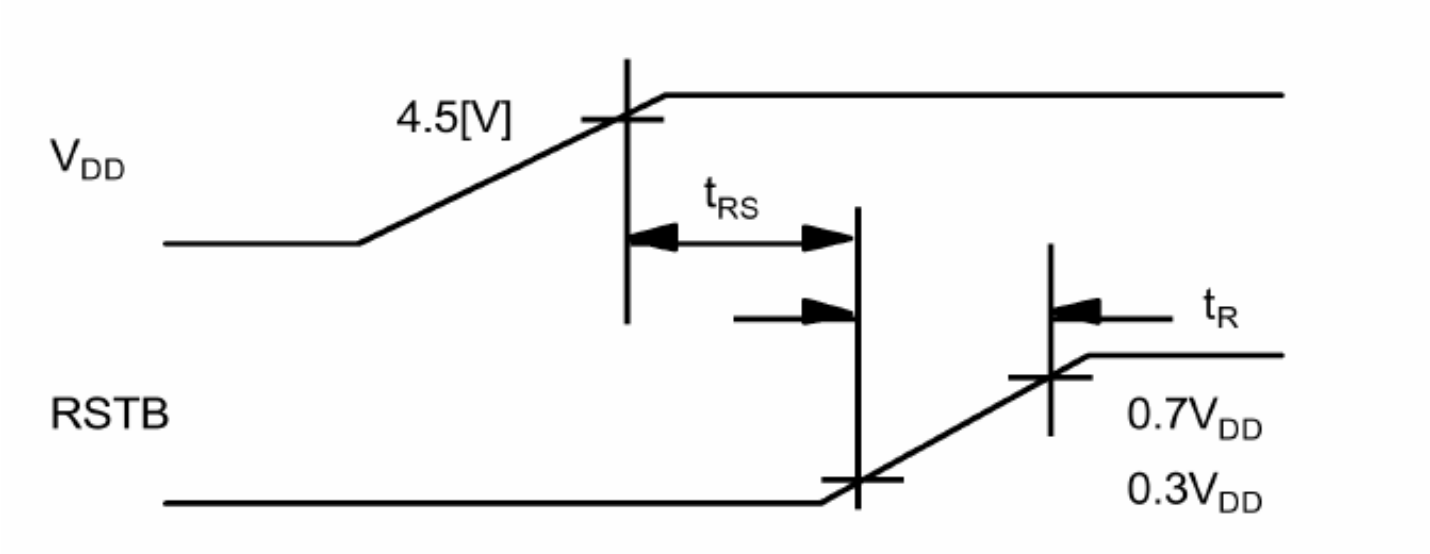
The system can be initialized by setting the RSTB to LOW when turning the power ON or by instruction from the MPU. When the RSTB is set to LOW, the following condition occurs:

1. The Display is turned OFF.
2. The Display Start Line register is set to 0 (Z-Address 0).

No instructions except the status read can be executed when the RSTB is LOW. This means that in order to execute other instructions, the RSTB must be cleared by setting DB4 to 0 and the DB7 set to 0 by status read instruction.

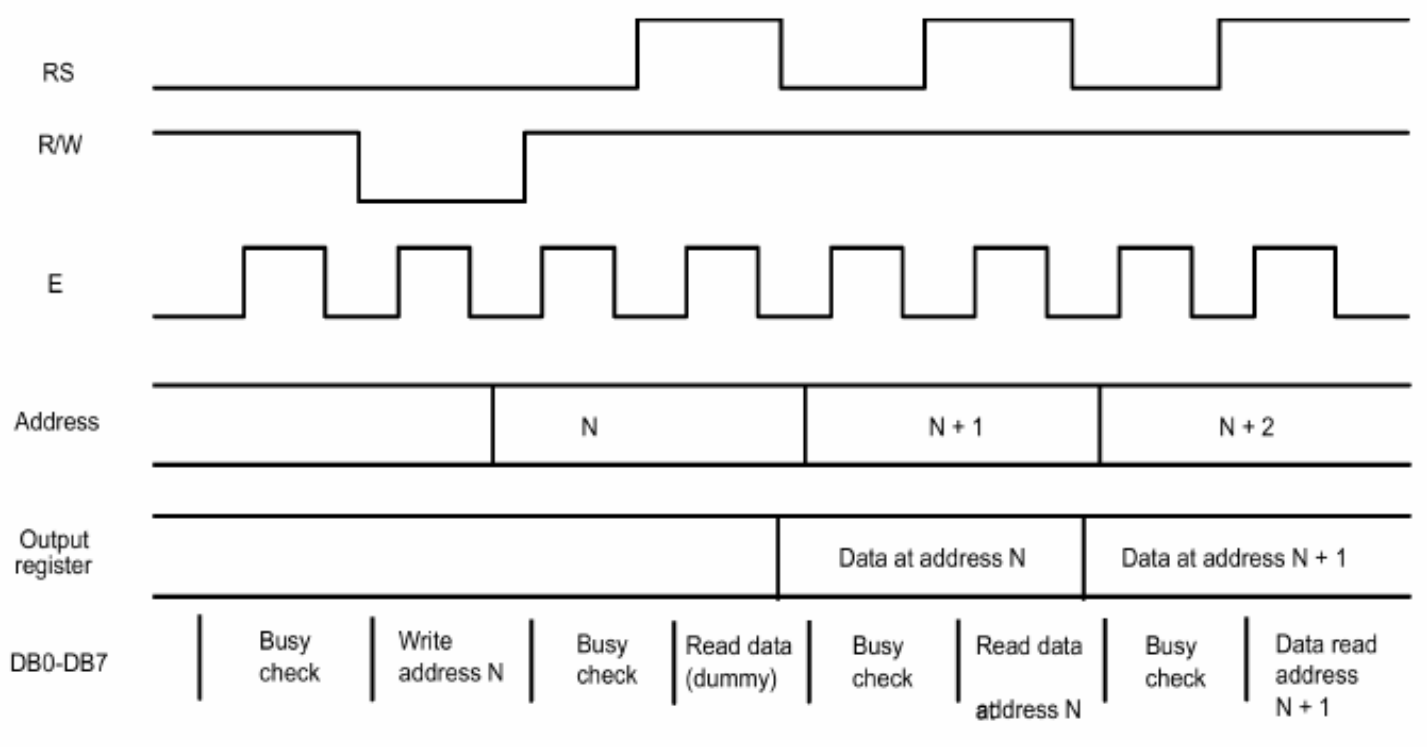
The table below shows the power supply initial conditions.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Reset Time	tRS	1.0	-	-	uS
Rise Time	tR	-	-	200	nS

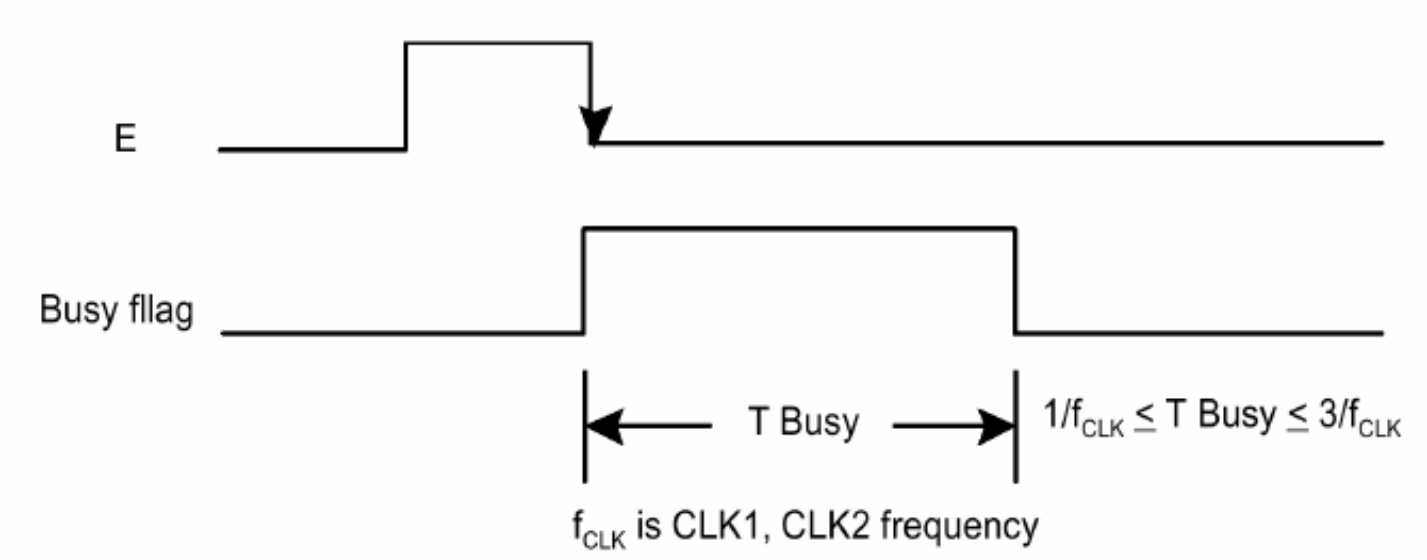


BUSY FLAG

The busy flag (DB7) is used to determine whether PT6608 is operating or not. When the busy flag is HIGH, internal operation is taking place. When the busy flag is LOW, PT6608 can accept data or instructions. The busy check diagram is shown below.



The busy flag diagram is shown below.



DISPLAY ON/OFF FLIP-FLOP

The Display On/Off Flip/Flop is used to turn the liquid crystal display ON or OFF. When the flip-flop is rest (or set to LOW), selective voltage or non-selective voltage appears on the segment output terminals. When the flip-flop is set to HIGH, non-selective voltage appears on the segment output terminals regardless of the display data RAM.

The Display On/Off Flip-Flop is synchronized with the CL signal and can change its status via instruction. The display data at all segments are cleared when RSTB is LOW. The status of the flip-flop is outputted to the DB5 by the status read instruction.

X PAGE REGISTER

The X page Register is used to determine the pages of the internal display data RAM. Count function is not available and address is set by instruction.

Y ADDRESS COUNTER

The Y Address Counter is used to designate the address of the internal display data RAM. The address is set by instruction and is increased by 1 automatically by the read or write operations of the display data.

DISPLAY DATA RAM

The Display Data RAM is used to store the display data for the liquid crystal display. Write data 1 is indicates an ON State of the LCDs dot matrix while the OFF State is written as 0. ADC Signal can control the Display Data RAM and the segment output. Please refer to the table below.

ADC *	Display Data
H	Y-Address 0:S1 to Y-Address 63:S64
L	Y-Address 0:S64 to Y-Address 63:S1

Note: * = ADC may be connected to VDD or Vss.

DISPLAY START LINE REGISTER

The Display Start Line Register is used to determine which display data RAM is to be displayed in the top line of the liquid crystal display. The bit data (DB0 to DB 5) of the display start line set instruction is latched in the display start line register. The latched data is then transferred to the Z-Address counter when FRM is “HIGH”, thereby presetting the Z-Address counter.

DISPLAY CONTROL INSTRUCTION

The internal state of PT6608 is controlled by the display control instructions which are sent by the MPU. Please refer to the table below.

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
DISPLAY ON/OFF	L	L	L	L	H	H	H	H	H	L/H	Controls the DISPLAY ON or OFF. Internal status and display RAM data are not affected. L:OFF, H:ON
SET ADDRESS (Y-ADDRESS)	L	L	L	H	Y-ADDRESS (0 ~ 63)						Sets the Y-address in the Y counter.
SET PAGE (X-ADDRESS)	L	L	H	L	H	H	H	PAGE (0 ~ 7)			Sets the X-address in the X-address register
DISPLAY START LINE (Z-ADDRESS)	L	L	H	H	DISPLAY START LINE (0 ~ 63)						Determines the display data RAM displayed at the top of the screen
STATUS READ	L	H	BUSY	L	ON/OFF	RESET	L	L	L	L	Reads status BUSY : L=READY H=IN OPERATION ON/OFF: L=DISPLAY ON H=DISPLAY OFF RESET: L=NORMAL H=RESET
WRITE DISPLAY DATA	H	L	WRITE DATA								Writes data (DB0 to DB7) to the display data RAM. After writing instruction, Y-address is automatically incremented by 1.
READ	H	H	READ DATA								Reads data (DB0 to DB7) from display data RAM to the data bus.

DISPLAY ON/OFF

The Display ON/OFF instruction is shown below:

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

DB0 is given the value of D. When D is “1”, the display data appears on the screen. When D is “0”, the display data is not shown on the screen; however, the display data is still present in the Display Data RAM. Thus, by changing D=”0” to D=”1”, the display data can reappear.

SET ADDRESS (Y-ADDRESS)

The Set Address instruction is shown below:

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

The Display Data RAM’s Y-Address (AC0 to AC5) is set in the Y-Address Counter. AC0 to AC5 are set by instruction and are automatically incremented by 1 by the read or write operations.

SET PAGE (X-ADDRESS)

The Set Page instruction is shown below:

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

The Display Data RAM’s X-Address (AC0 to AC2) are set in the X-Address counter. Writing or reading to or from the MPU is executed in this specified page until the next page is set.

STATUS READ

The Status Read instruction is shown below:

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	0	ON/OFF	RESET	0	0	0	0

BUSY

When BUSY is “1”, no instructions can be accepted since PT6608 is busy executing an internal operation. When BUSY is “0”, PT6608 is ready to accept any instruction.

ON/OFF

When the ON/OFF is “1”, display is turned ON. Conversely, when ON/OFF is “0”, display is turned OFF.

RESET

When RESET is “1”, the system is being restarted or initialized. Under this condition, with the exception of the Status Read instruction, no instructions can be accepted. When RESET is “0”, the reset or initializing operation has been completed and the system is in its normal operating condition.

WRITE DISPLAY DATA

The Write Display Data instruction is shown below:

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

The data bits D0 to D7 are written into the Display Data RAM. After writing instruction is completed, the Y-Address is incremented automatically by 1.

READ DISPLAY DATA

The Read Display Data instruction is shown below:

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

The data bits D0 to D7 are read from the Display Data RAM. After the reading operation is completed, the Y-Address is incremented automatically by 1.

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Operating Voltage **(see Note 1)**	VDD	-0.3 to +7.0	V
Supply Voltage **(see Note 4)**	VEE	VDD -19.0 to VDD +0.3	V
Driver Supply Voltage	VB	-0.3 to VDD +0.3 **(see Notes 1 & 3)**	V
	VLCD	VEE -0.3 to VDD +0.3 **(see Note 2)**	V
Operating Temperature	TOPR	-30 to +85	°C
Storage Temperature	TSTG	-55 to +125	°C

Notes:

1. Based on VSS=0V
2. Applies the same supply voltage to VEE1 and VEE2. VLCD=VDD-VEE
3. Applies to M, FRM, CL, RSTB, ADC, CLK1, CLK2, CS1B, CS2B, CS3, E, R/W, RS and DB0 to DB7
4. Applies to V0L, V0R, V2L, V2R. V3L, V3R, V5L, and V5R.
   Voltage Level: VDD ≥ V0L=V0R ≥ V2L=V2LR ≥ V3L=V3R ≥ V5L=V5R ≥ VEE

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD= +5V ± 10%, VSS=0V, VDD-VEE =8 to 17V, Ta=-30 to +85 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High Level Input Voltage	VIH1	**(see Note 1)**	0.7VDD	-	VDD	V
	VIH2	**(see Note 2)**	0.7VDD		VDD	V
Low Level Input Voltage	VIL1	**(see Note 1)**	0	-	0.3VDD	V
	VIL2	**(see Note 2)**	0		0.8	V
High Level Output Voltage	VOH	IOH = -200 μA **(see Note 3)**	2.4	-	-	V
Low Level Output Voltage	VOL	IOL = 1.6 mA **(see Note 3)**	-	-	0.4	V
Input Leakage Current	ILKG	VIN = VDD to VSS **(see Note 4)**	-1.0	-	1.0	μA
Three-State (OFF) Input Current	ITSL	VIN = VDD to VSS **(see Note 5)**	-5.0	-	5.0	μA
Driver Input Leakage Current	IDIL	VIN = VEE to VSS **(see Note 6)**	-2.0	-	2.0	μA
Operating Current	IDD1	During Display **(see Note 7)**	-	-	100	μA
	IDD2	During Access, Access Cycle = 1MHz **(see Note 8)**	-	-	500	μA
On Resistance	Ron	VDD - VEE = 15V ILOAD = ± 0.1mA **(see Note 8)**	-	-	7.5	kOhms

Notes:

1. CL, FRM, M, RSTB, CLK1, CLK2
2. CS1B, CS2B, CS3, E, R/W, RS, DB0 to DB7
3. DB0 to DB7
4. Except DB0 to DB7
5. DB0 to DB7 at High Impedance
6. V0L, V0R, V2L, V2R, V3L, V3R, V5L, V5R
7. 1/64 duty, FCLK = 250 kHz, Frame Frequency = 70Hz, output: No Load
8. VDD-VEE = 15.5V
   VOL(R) > V2L(R) = VDD-2/7 (VDD - VEE) > V3L(R) = VEE + 2/7 (VDD - VEE) > V5L(R)

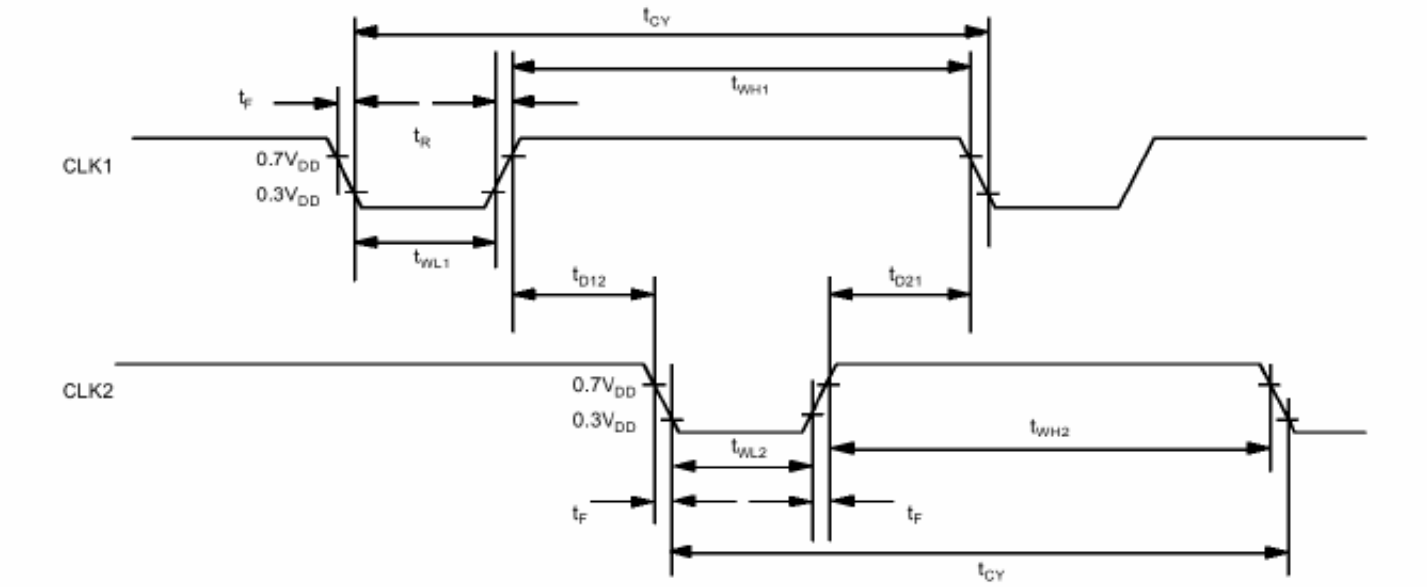
AC CHARACTERISTICS

(VDD=5V ± 10%, VSS=0V, Ta=-30 °C to +85 °C)

CLOCK TIMING

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK1, CLK2 Cycle Time	tCY	2.5	-	20	µs
“CLK1” “LOW” “Level Width”	tWL1	625	-	-	ns
“CLK2” “LOW” “Level Width”	tWL2	625	-	-	ns
“CLK1” “HIGH” “Level Width”	tWH1	1875	-	-	ns
“CLK2” “HIGH” “Level Width”	tWH2	1875	-	-	ns
CLK1 - CLK2 Phase Difference	tD12	625	-	-	ns
CLK2 - CLK1 Phase Difference	tD21	625	-	-	ns
CLK1, CLK2 Rise Time	tR	-	-	150	ns
CLK1, CLK2 Fall Time	tF	-	-	150	n

The external clock waveform diagram is given below.



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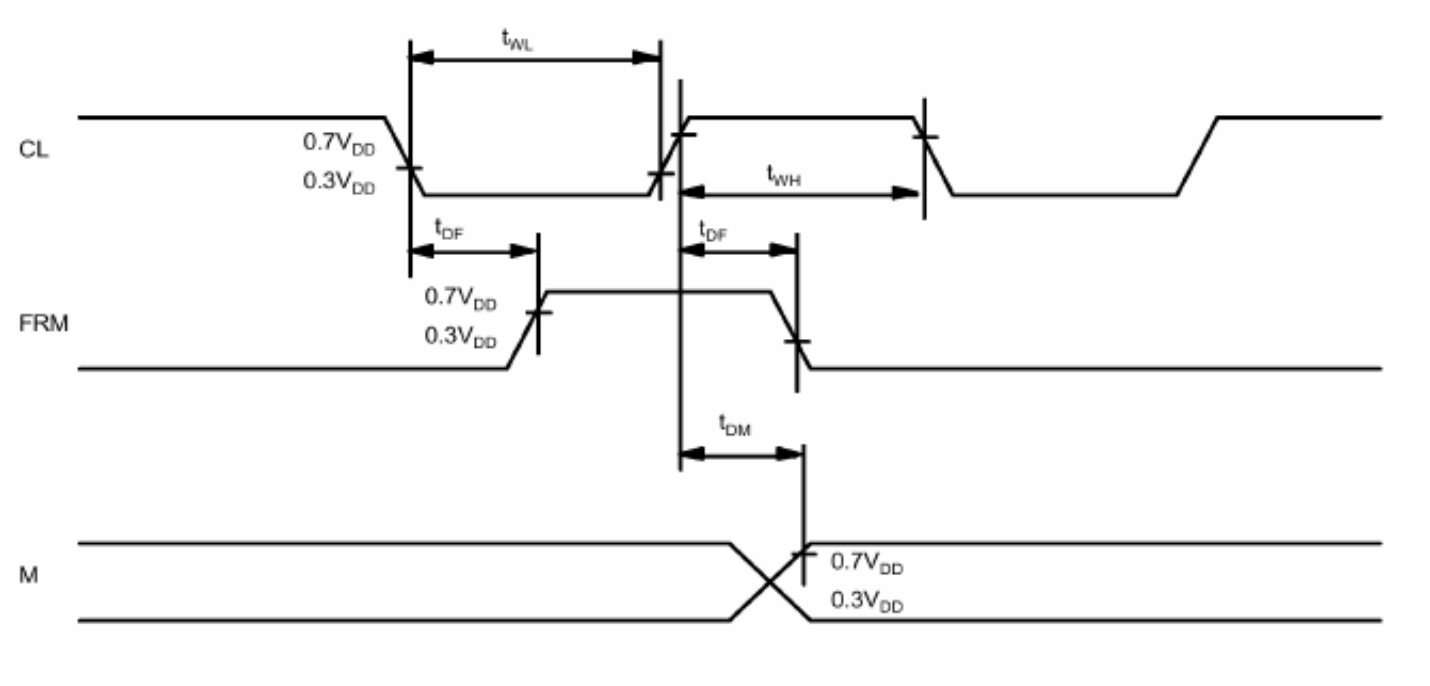
DISPLAY CONTROL TIMING

Parameter	Symbol	Min.	Typ.	Max.	Unit
FRM Delay Time	tDF	-2	-	+2	µs
M Delay Time	tDM	-2	-	+2	µs
“CL” “LOW” “Level Width”	tWL	35	-	-	µs
“CL” “HIGH” “Level Width”	tWH	35	-	-	µ

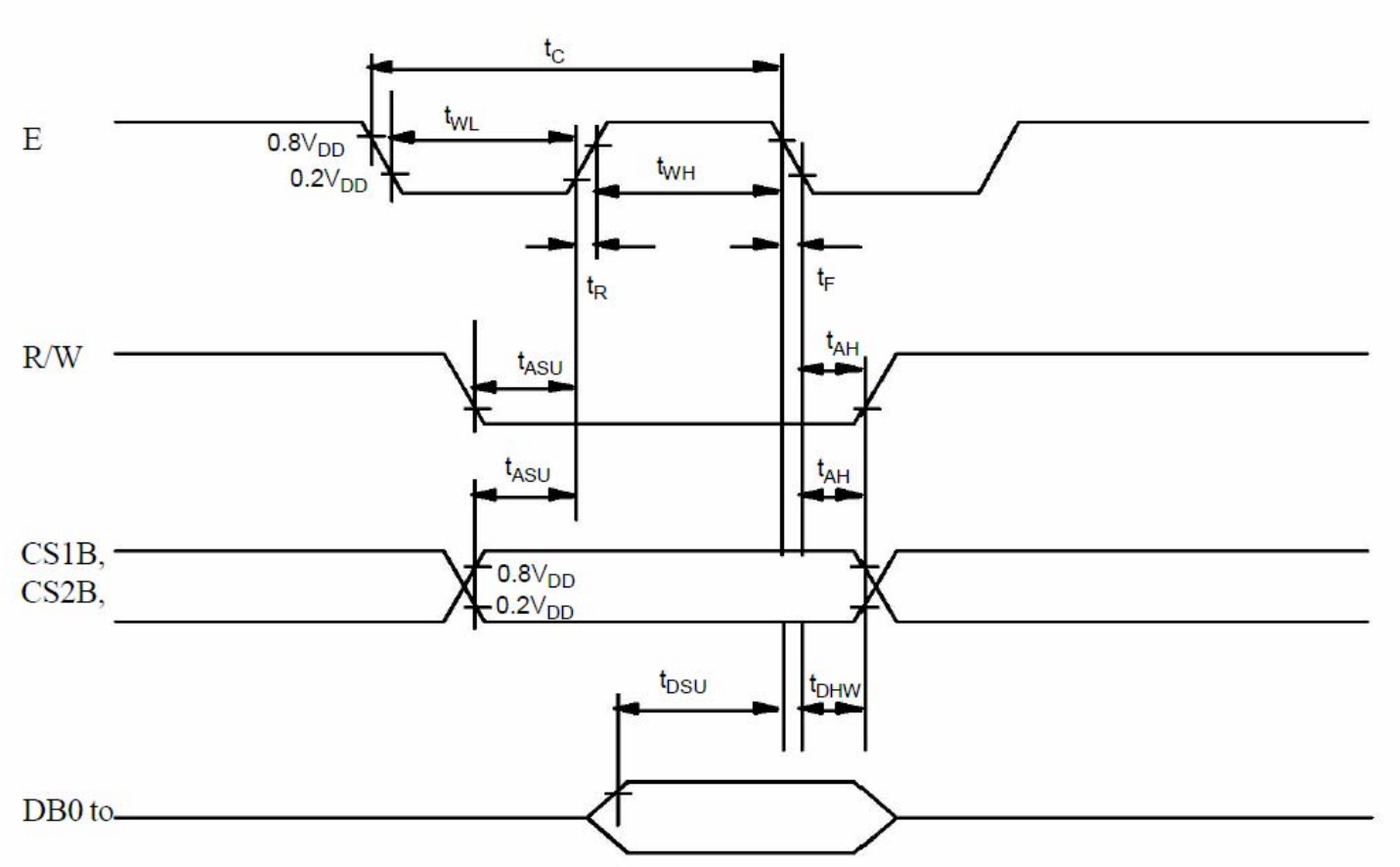
The display control signal waveform is given below.



MCU INTERFACE

Parameter	Symbol	Min.	Typ.	Max.	Unit
E Cycle	tC	1000	-	-	ns
E High Level Width	tWH	450	-	-	ns
E Low Level Width	tWL	450	-	-	ns
E Rise Time	tR	-	-	25	ns
E Fall Time	tF	-	-	25	ns
Address Set-up Time	tASU	140	-	-	ns
Address Hold Time	tAH	10	-	-	ns
Data Set-up Time	tSU	200	-	-	ns
Data Delay Time	tD	-	-	320	ns
Data Hold Time (Write)	tDHW	10	-	-	ns
Data Hold Time (Read)	tDHR	20	-	-	n

The MPU write timing waveform is given below.



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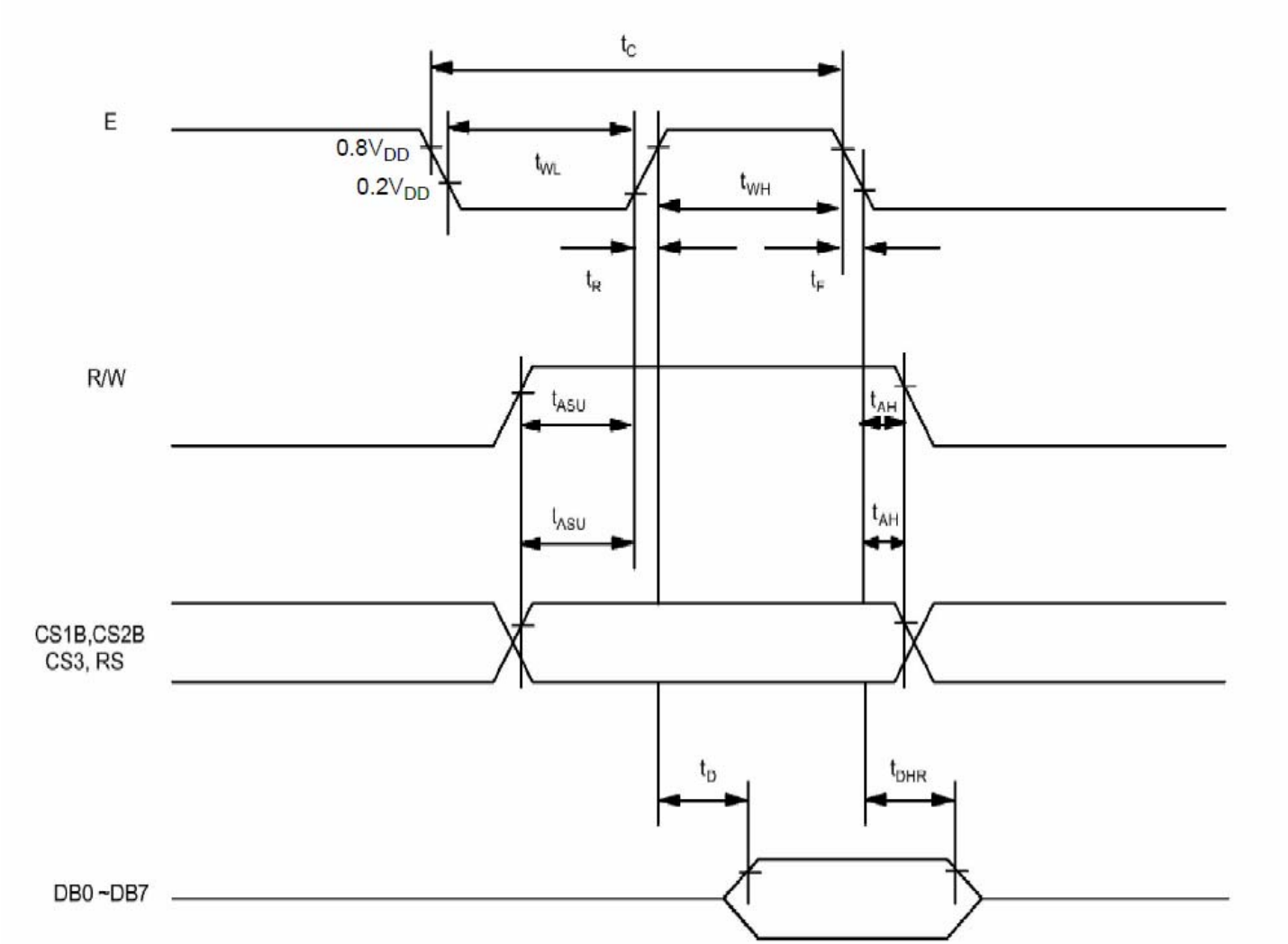
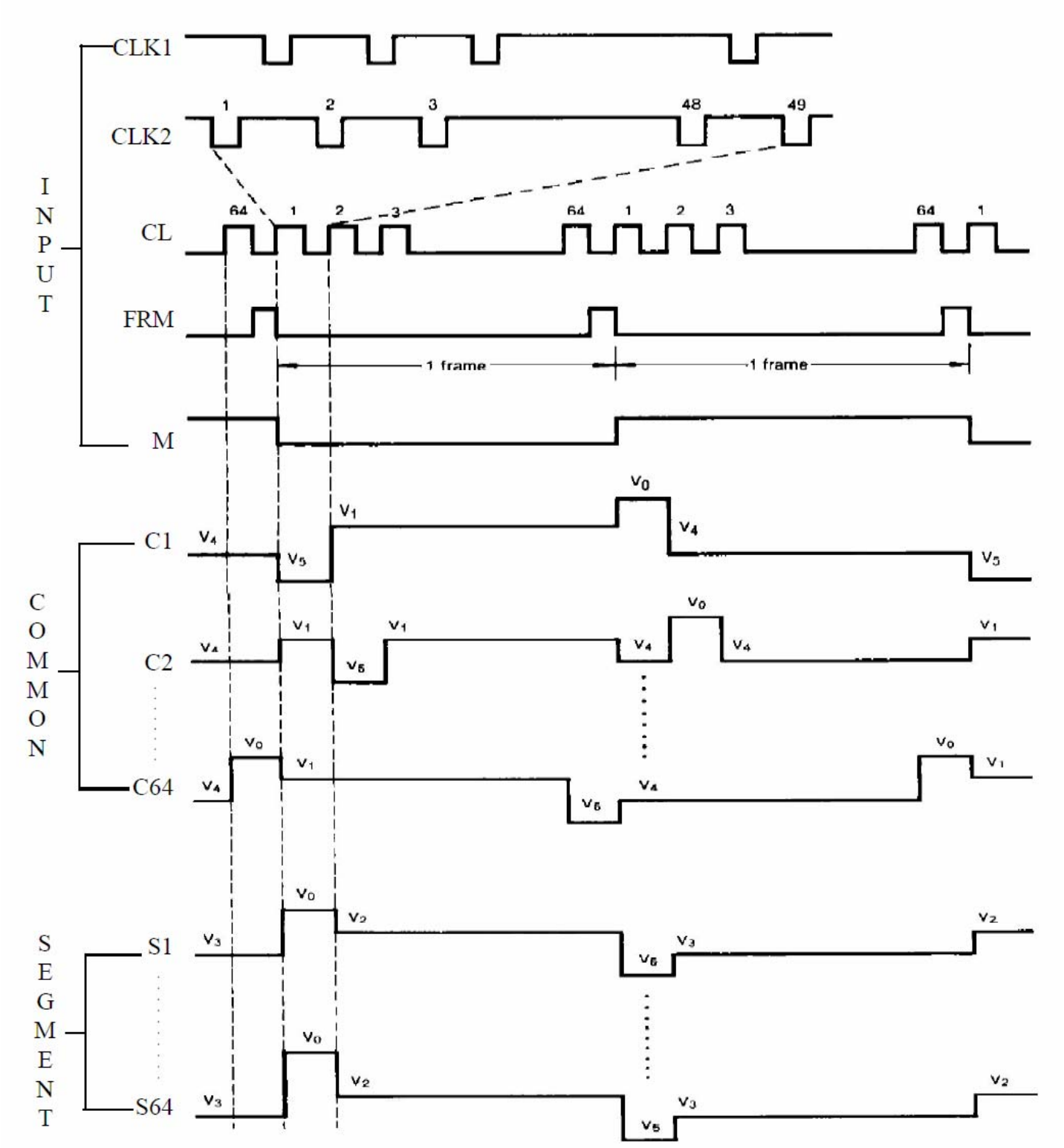
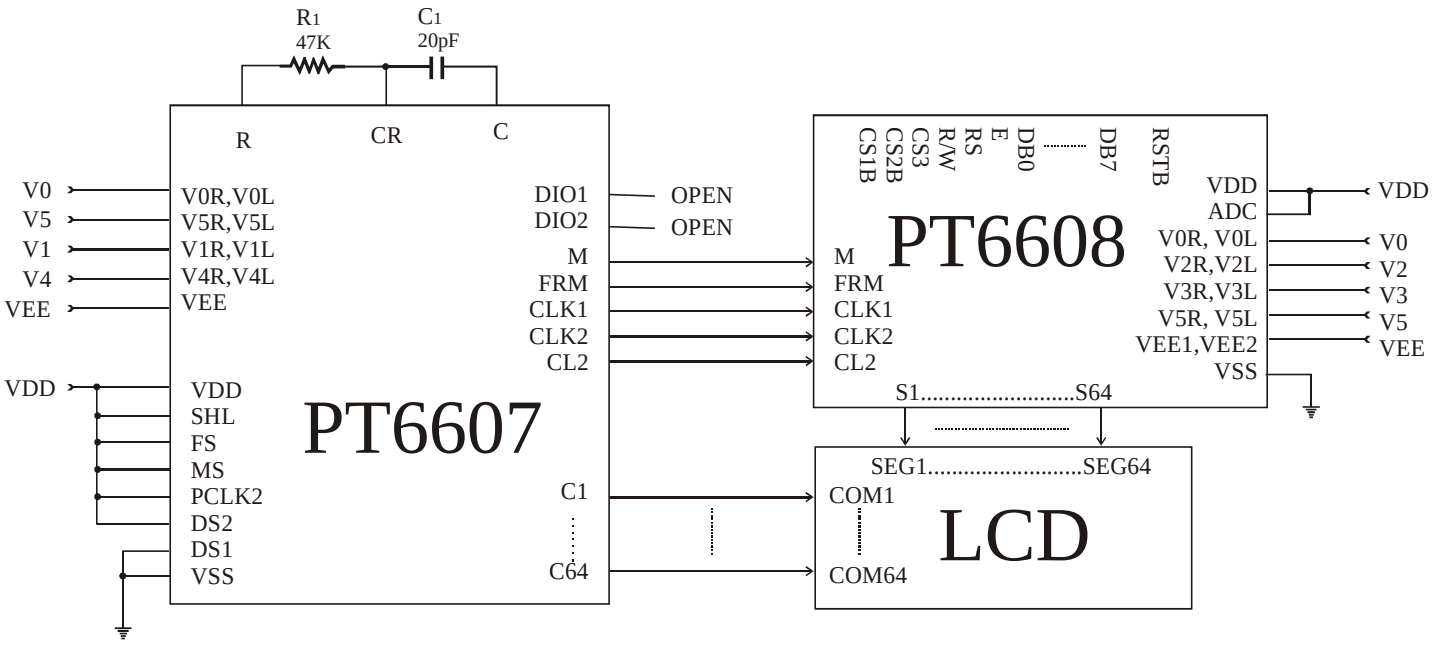
The MPU read timing waveform is shown below.



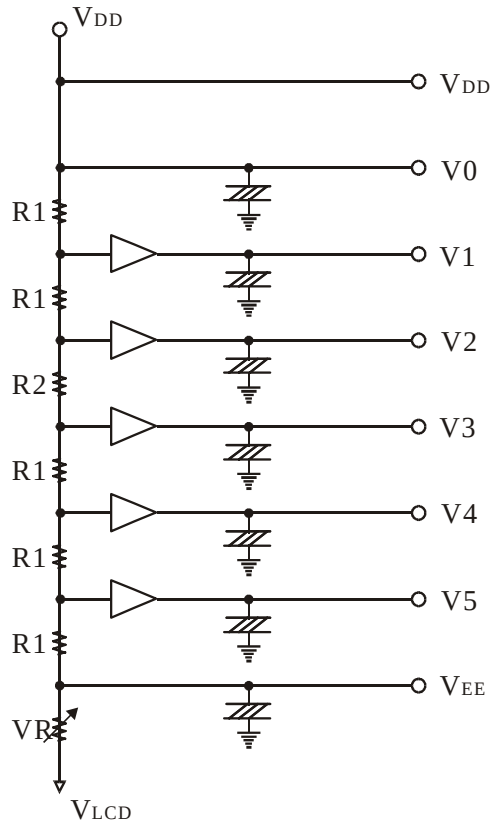
1/64 DUTY TIMING DIAGRAM



APPLICATION CIRCUIT



POWER DRIVER CIRCUIT



Duty	Bias	Rdiv
1/48	1/8	R2=4R1
1/64	1/9	R2=5R1
1/96	1/11	R2=7R1
1/128	1/12	R2=8R1

Notes:

1. When the duty factor is 1/48, the value of R1 and R2 must satisfy the following:
   R1/(4R1+R2)=1/8
   R1=3 k
   R2=12 k

2. Bias means division of voltage between VDD and VEE.
   Ex. 1/8 Bias means divide the voltage VDD and VEE to be 8 equalizers.

3. V1, V2, V3, V4, V5 and VEE voltage levels can be adjusted by the VR.

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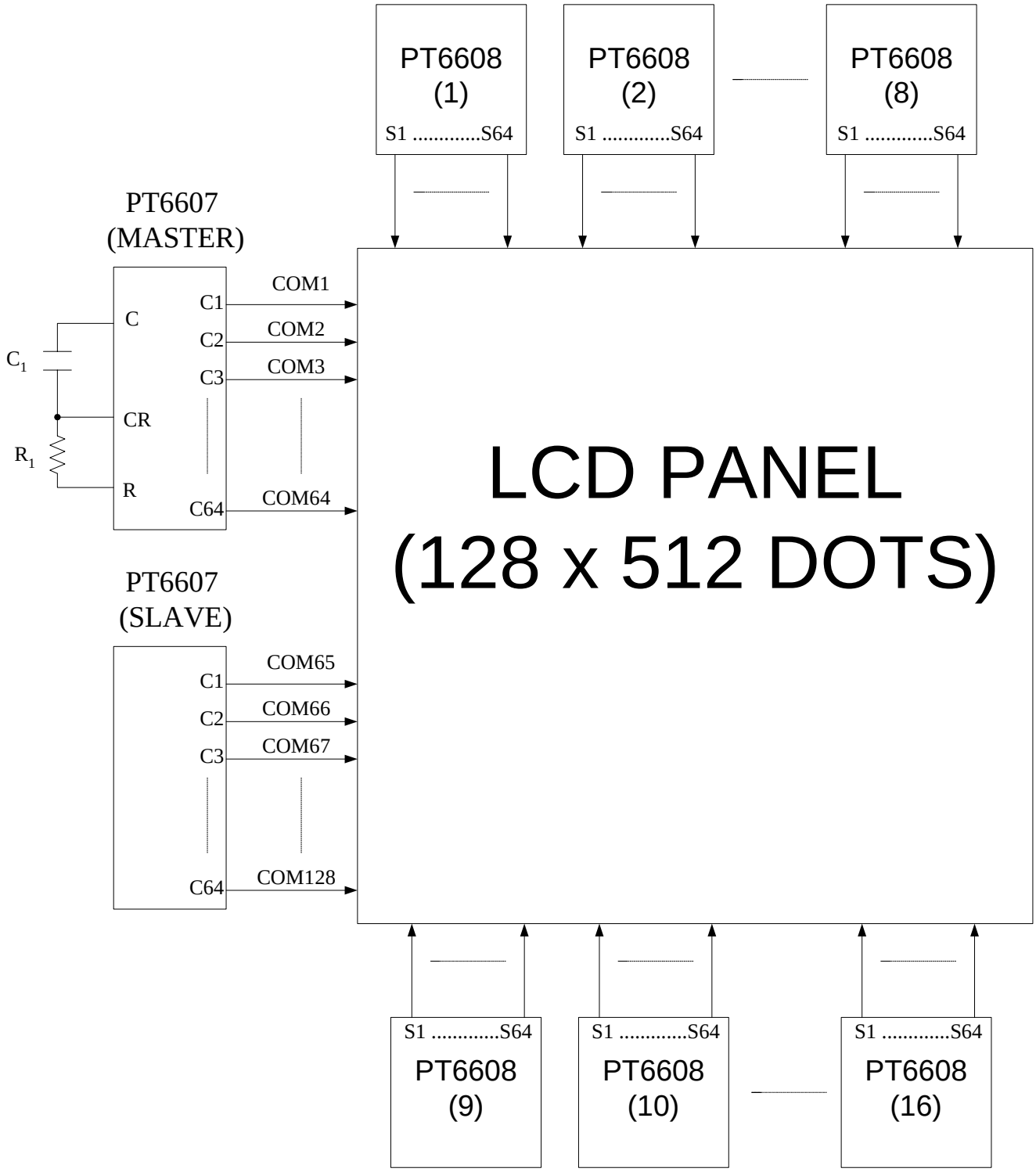
LCD PANEL INTERFACE APPLICATION CIRCUIT



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ORDER INFORMATION

Valid Part Number	Package Type
PT6608	100-pin QFP
PT6608-H	C.O.B

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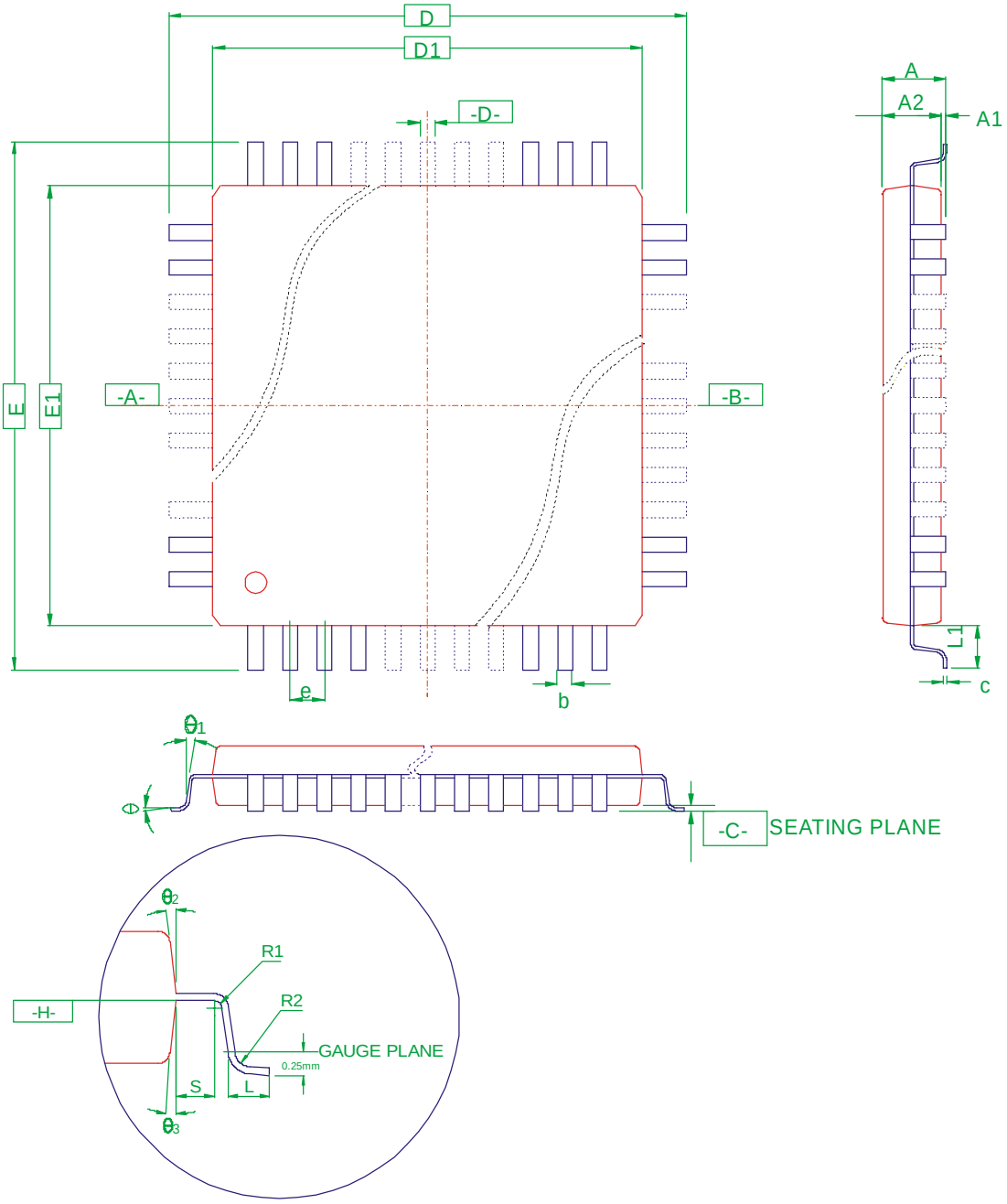
PACKAGE INFORMATION

100-PIN QFP (BODY SIZE: 20MM X 14MM, PITCH: 0.65MM)



Symbol	Min.	Nom.	Max
c	0.11	-	0.23
L	0.73	0.88	1.03
L1	-	1.60	-
A	-	-	3.40
A1	0.25	-	0.50
A2	2.50	2.70	2.90
b	0.22	-	0.40
R1	0.13	-	-
R2	0.13	-	0.30
q	0°	-	7o
q1	0°	-	-
q2	5°	-	16°
q3	5°	-	16°
S	0.20	-	-
D	23.20 BASIC		
D1	20.00 BASIC		
E	17.20 BASIC		
E1	14.00 BASIC		
e	0.65 BASIC		

Notes:

1. All dimensioning and tolerancing conform to ASME Y14.5M-1994
2. Dimensions D1 and E1 do not include mold protrusion, allowable protrusion is 0.25 mm per side, dimensions D1 and E1 do include mold mismatch and are determined at datum plane H".
3. Details of Pin 1 identifier are optional but must be located within the zone indicated.
4. Regardless of the relative size of the upper and lower body sections, dimensions D1 and E1 are determined at the largest feature of the body exclusive of mold flash and gate burrs but including any mismatch between the upper and lower sections of the molded body.
5. All dimensions are in millimeters.
6. Dimension b do not include dambar protrusion. The dambar protrusion(s) shall not cause the lead width to exceed B maximum by more than 0.08 mm. Dambar cannot be located on the lower radius or the lead foot.
7. A1 is defined as the distance from the seating plane to the lowest point of the package body.
8. Refer to JEDEC MS-022 Variation GC-1.

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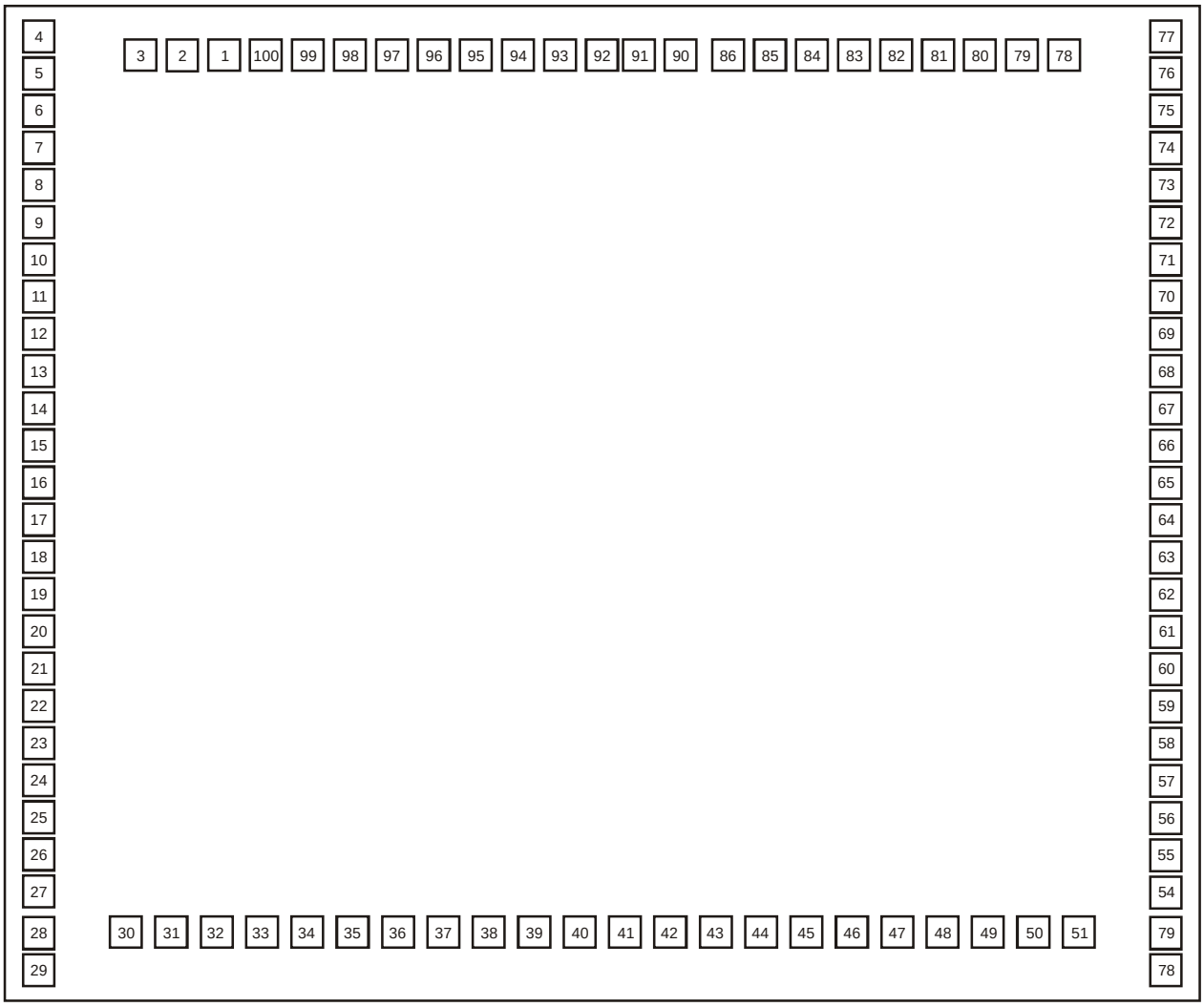
PAD CONFIGURATION



Chip Size: 3355.6 x 3035.9 μm
Pad Size: 90 x 90 μm
Pitch: 110 μm

Note: * = The dice substrate is an n-substrate; therefore, it is recommended that it be connected to VDD. If it is connected to VSS, then there is a great possibility that the chip will be damaged.

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PAD LOCATION

Pad No.	Pad Name	Location
1	ADC	[648.300, 2870.500]
2	M	[538.300, 2870.500]
3	VCC	[424.400, 2870.500]
4	V3	[73.900, 2930.000]
5	V2	[73.900, 2805.000]
6	V5	[73.900, 2680.000]
7	V0	[73.900, 2555.000]
8	VEE	[73.900, 2440.000]
9	S(64)	[73.900, 2330.000]
10	S(63)	[73.900, 2220.000]
11	S(62)	[73.900, 2110.000]
12	S(61)	[73.900, 2000.000]
13	S(60)	[73.900, 1890.000]
14	S(59)	[73.900, 1780.000]
15	S(58)	[73.900, 1670.000]
16	S(57)	[73.900, 1560.000]
17	S(56)	[73.900, 1450.000]
18	S(55)	[73.900, 1340.000]
19	S(54)	[73.900, 1230.000]
20	S(53)	[73.900, 1120.000]
21	S(52)	[73.900, 1010.000]
22	S(51)	[73.900, 900.000]
23	S(50)	[73.900, 790.000]
24	S(49)	[73.900, 680.000]
25	S(48)	[73.900, 570.000]
26	S(47)	[73.900, 460.000]
27	S(46)	[73.900, 330.000]
28	S(45)	[73.900, 200.000]
29	S(44)	[73.900, 70.000]
30	S(43)	[483.200, 208.600]
31	S(42)	[593.200, 208.600]
32	S(41)	[703.200, 208.600]
33	S(40)	[813.200, 208.600]
34	S(39)	[923.200, 208.600]
35	S(38)	[1033.200, 208.600]
36	S(37)	[1143.200, 208.600]
37	S(36)	[1253.200, 208.600]
38	S(35)	[1363.200, 208.600]
39	S(34)	[1473.200, 208.600]
40	S(33)	[1583.200, 208.600]

Pad No.	Pad Name	Location
41	S(32)	[1772.400, 208.600]
42	S(31)	[1882.400, 208.600]
43	S(30)	[1992.400, 208.600]
44	S(29)	[2102.400, 208.600]
45	S(28)	[2212.400, 208.600]
46	S(27)	[2322.400, 208.600]
47	S(26)	[2432.400, 208.600]
48	S(25)	[2542.400, 208.600]
49	S(24)	[2652.400, 208.600]
50	S(23)	[2762.400, 208.600]
51	S(22)	[2872.400, 208.600]
52	S(21)	[3281.700, 70.000]
53	S(20)	[3281.700, 200.000]
54	S(19)	[3281.700, 330.000]
55	S(18)	[3281.700, 460.000]
56	S(17)	[3281.700, 570.000]
57	S(16)	[3281.700, 680.000]
58	S(15)	[3281.700, 790.000]
59	S(14)	[3281.700, 900.000]
60	S(13)	[3281.700, 1010.000]
61	S(12)	[3281.700, 1120.000]
62	S(11)	[3281.700, 1230.000]
63	S(10)	[3281.700, 1340.000]
64	S(9)	[3281.700, 1450.000]
65	S(8)	[3281.700, 1560.000]
66	S(7)	[3281.700, 1670.000]
67	S(6)	[3281.700, 1780.000]
68	S(5)	[3281.700, 1890.000]
69	S(4)	[3281.700, 2000.000]
70	S(3)	[3281.700, 2110.000]
71	S(2)	[3281.700, 2220.000]
72	S(1)	[3281.700, 2330.000]
73	VEE	[3281.700, 2440.000]
74	V0	[3281.700, 2555.000]
75	V5	[3281.700, 2680.000]
76	V2	[3281.700, 2805.000]
77	V3	[3281.700, 2930.000]
78	GND	[2947.400, 2870.500]
79	DB(0)	[2821.600, 2870.400]
80	DB(1)	[2699.700, 2870.400]
81	DB(2)	[2577.800, 2870.400]
82	DB(3)	[2455.900, 2870.400]
83	DB(4)	[2334.000, 2870.400]

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Pad No.	Pad Name	Location
84	DB(5)	[2212.100, 2870.400]
85	DB(6)	[2090.200, 2870.400]
86	DB(7)	[1968.300, 2870.400]
87	NC	[1858.300, 2870.500]
88	NC	[1748.300, 2870.500]
89	NC	[1638.300, 2870.500]
90	CS3	[1858.300, 2870.500]
91	CS2B	[1748.300, 2870.500]
92	CS1B	[1638.300, 2870.500]
93	RSTB	[1528.300, 2870.500]
94	RW	[1418.300, 2870.500]
95	RS	[1308.300, 2870.500]
96	CL	[1198.300, 2870.500]
97	CLK2	[1088.300, 2870.500]
98	CLK1	[978.300, 2870.500]
99	E	[868.300, 2870.500]
100	FRM	[758.300, 2870.500]