GRAFIKKONTROLLER

T6963C is newest Thoshiba's LSI for a large scale dot matrix LCD in CMOS process. It is designed to construct a low power LCD module by combining together with T6961A (LCD drive LSi's). T6963C can support a very board range of LCD dots by combinations of programmable inputs.
T6963C can be used in every cases of character mode, graphic mode and combination mode of character and graphic, and has various attribute functions.
T6963C has 8-bits parallel bus for reading/writing data by CPU interface.
During reading or writing data by CPU I/F, any noise doesn't appear in display screen. It has internally 128 words character generator ROM. It has also capability to control external display RAM in size upto 64k byte, and can be classified freely to ranges of text, graphic and external character generator, and can freely transfer the position of display window.
T6963C transfers display data to driver LSI's serially by 2 methods. The first is the method to use one serialdata line, and the second is the method to use two serial lines for odd dots and even dots, so that it is easy to connect lines between LCD panel and driver LSI's on the LCD PCB.

--- FEATURES ---

* Selection of display size by program inputs

  columns : 32, 40, 64, 80

  lines : 2, 4, 6, 8, 10, 12, 14, 16 x 1 screen or
  x 2 screens

  dots per font: horizontal dots 5, 6, 7, 8
  vertical dots 8

  display duty: 1/16 to 1/128 (upto 256 dot lines when 2 areas are driven)

ELECTRONIC ASSEMBLY GMBH
LOCHHAMER SCHLAG 17 · D-82166 GRÄFELFING
TELEFON 089/8541991 · TELEFAX 089/8541721

* Internal 128 words character generator ROM
* External display memory: 64K byte MAX.
* No noise in display screen when CPU reads/writes the data of display memory.
* AND/OR/EX-OR functions of screen data between text and graphic
* Software programmable of text/graphic/external character generator ranges in display memory
* Software programmable of the positions of both text and graphic display windows
* Read and copy of the data of display screen
* Bit set and bit reset of display memory
* Verious attribute functions
  - Cursor pattern selectable
  - Cursor on/off/blink
  - Character on/off/blink
  - Character normal/inverse
* Asynchronous operation to CPU clock by internal crystal oscillator
* High speed operation
* Low power consumption
* Operating voltage: +5V

Absolute Maximum Ratings

ITEM	SYMBOL	CONDITION	RATING	UNIT
Supply Voltage	VDD	Ta=25°C	-0.3∿+7.0	V
Input Voltage	VIN	Ta=25°C	-0.3∿VDD+0.3	V
Operating temperature	Topr		-10∿+70	°C
Storage Temperature	Tstg		-55∿+125	°C

Note: Values measured at VSS=0V.

Electrical Characteristics
Test Conditions Unless Otherwise Specified, VSS=0V, VDD=+5V±10%, Ta=25°C

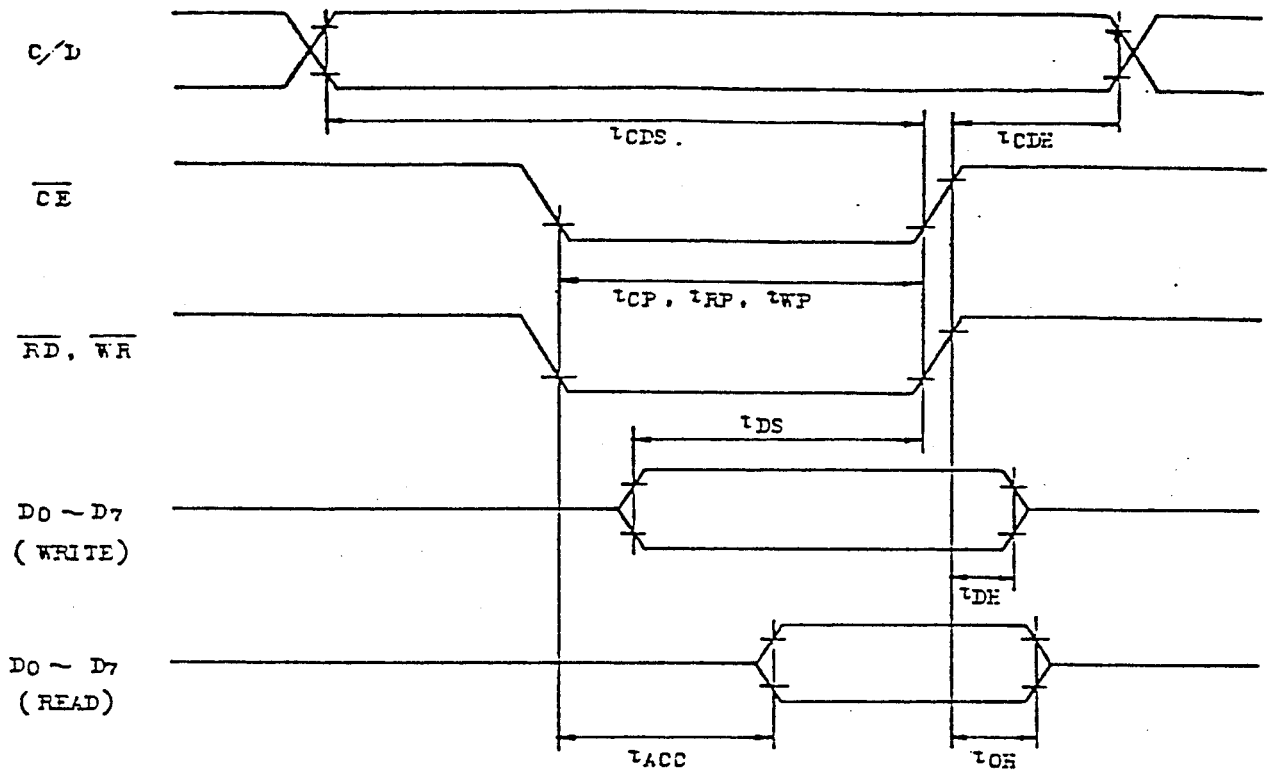
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	VDD		+4.5	+5.0	+5.5	V
"H" Input Voltage	VIH		VDD-2.2	-	VDD	V
"L" Input Voltage	VIL		0	-	+0.8	V
"H" Output Voltage	VOH		VDD-0.3	-	VDD	V
"L" Output Voltage	VOL		0	-	+0.3	V
"H" Output Resistance	ROH	VOUT=VDD-0.5V	-	-	400	Ω
"L" Output Resistance	ROL	VOUT=+0.5V	-	-	400	Ω
Input Pullup (note 1) Resistance	RPU		50	100	200	kΩ
Operating Frequency	Fosc		0.4	-	5.5	MHz
Current Consumption (Operating)	IDD1	VDD=5.0V (note 2)	-	3.3	6	mA
Current Consumption (Halt)	IDD2	VDD=5.0v	-	-	3	μA

(note 1): Applied $\overline{T1}$, $\overline{T2}$, $\overline{RESET}$

(note 2): MDS="L", MD0="L", MD1="L", MD2="H", MD3="H", FS0="L", FS1="L"
SDSEL="L", $\overline{DUAL}$="H", D7 0="LHLHLHLH"
fosc=3.0MHz

T6963C Switching Characteristics (1)

Bus Timing

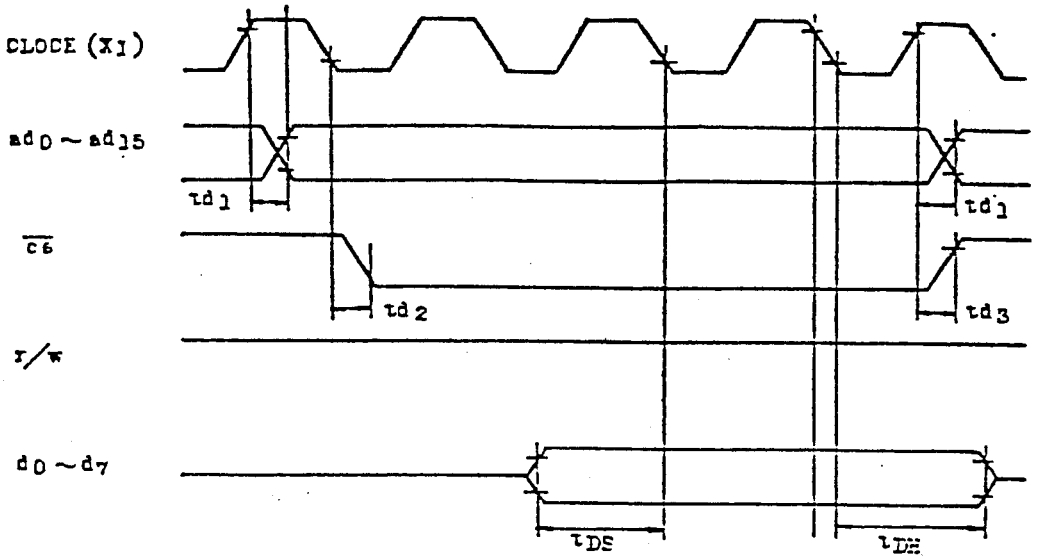


VDD=5V±10%, VSS=0V, Ta=-10 ~ +70 °C

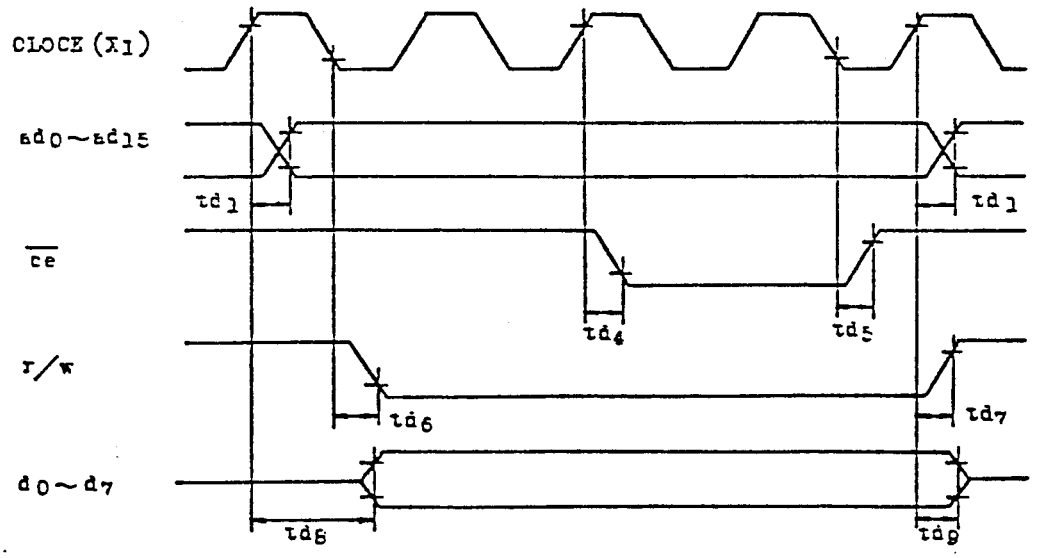
ITEM	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
C/D Set Up Time	tcds		100	-	ns
C/D Hold Time	tcdh		10	-	ns
CE,RD,WR Pulse Width	tcp trp twp		80	-	ns
Data Set Up Time	tds		80	-	ns
Data Hold Time	tdh		40	-	ns
Access Time	tacc		-	150	ns
Output Hold Time	toh		10	50	ns

T6963C Switching Characteristics (2)

(1) Read Mode



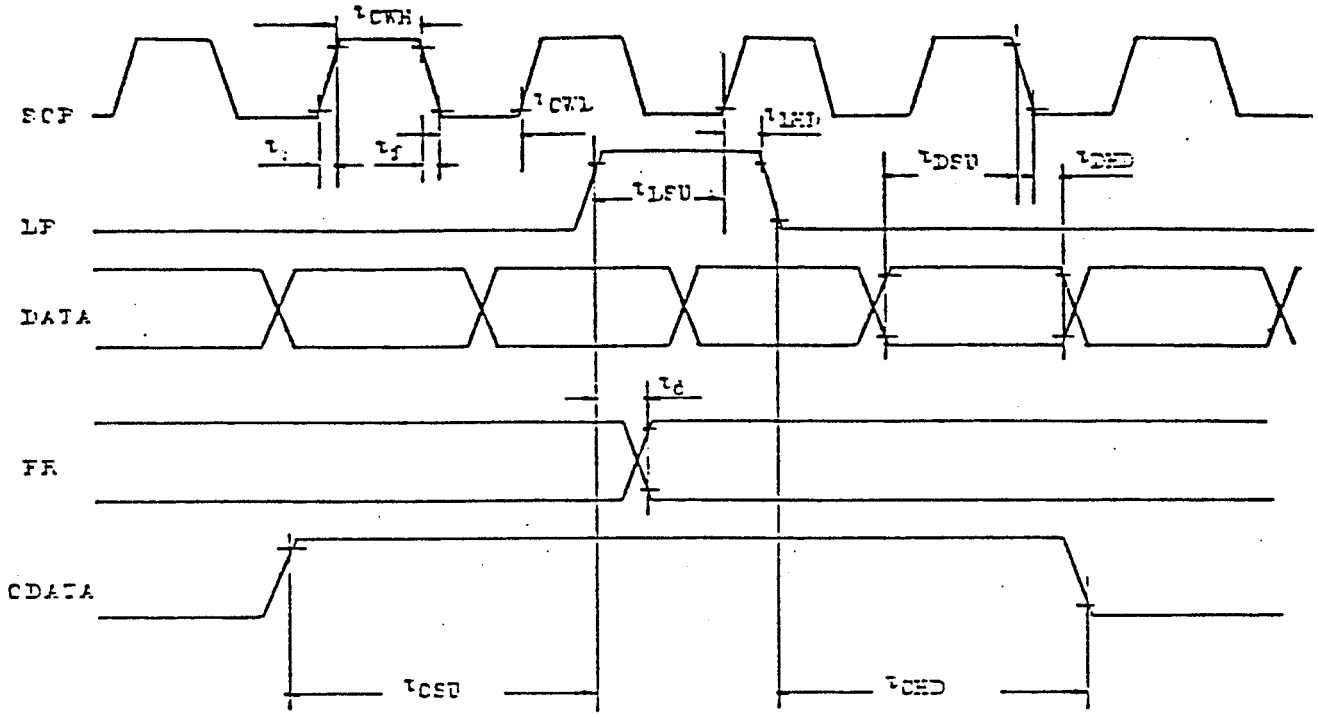
(2) Write Mode



VDD=5V±10%, VSS=0V, Ta=-10 ~ +70 °C

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Address Delay Time	td1		-	250	ns
$\overline{ce}$ Fall Delay Time(Read)	td2		-	180	ns.
$\overline{ce}$ Rise Delay Time(Read)	td3		-	180	ns
Data Set Up Time	tds		0	-	ns
Data Hold Time	tdh		30	-	ns
$\overline{ce}$ Fall Delay Time(Write)	td4		-	200	ns
$\overline{ce}$ Rise Delay Time(Write)	td5		-	200	ns
r/w Fall Delay Time	td6		-	180	ns
r/w Rise Delay Time	td7		-	180	ns
Data Stable Time	td8		-	450	ns
Data Hold Time	td9		-	200	ns

T6963C Switching Characteristics (3)



VSS=0V, VDD=+5V±10%

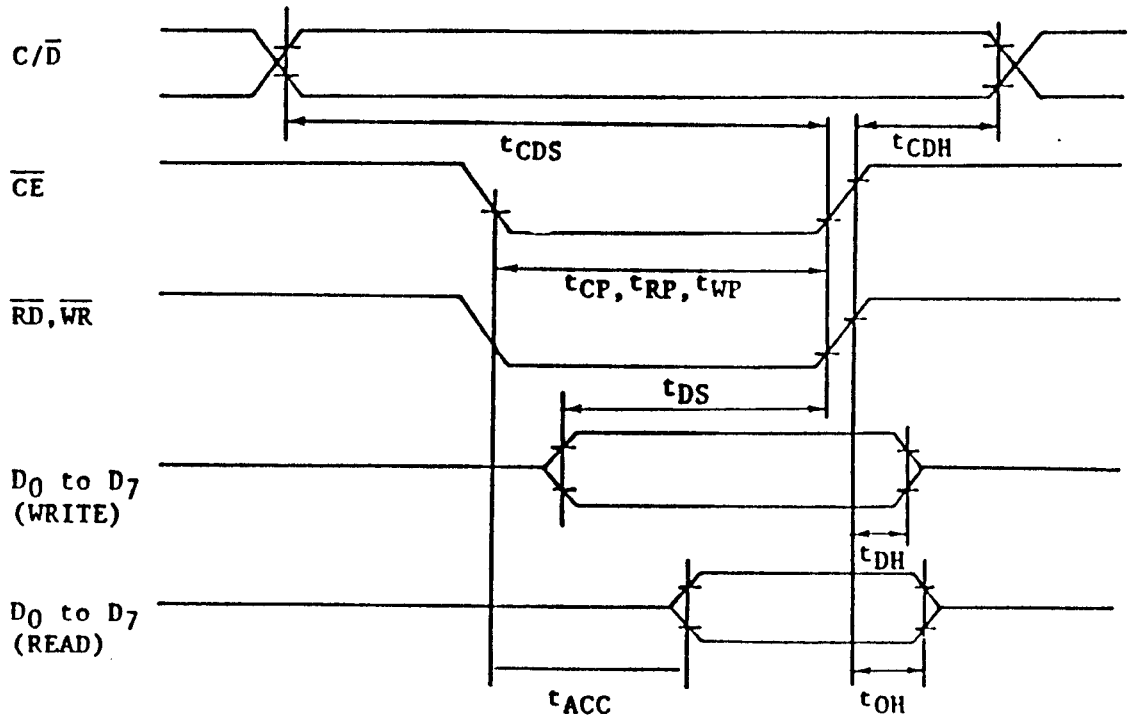
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Operating Frequency	fscp	Ta=-10 ∿ +70 °c	-	2.75	MHz
SCP Pulse Width	tcwh tcwl		150	-	ns
SCP Rise/Fall Time	tr tf		-	30	ns
LP Set Up Time	tlsu		150	290	ns
LP Hold Time	tlhd		5	40	ns
Data Set Up Time	tdsu		170	-	ns
Data Hold Time	tdhd		80	-	ns
FR Delay Time	td		0	90	ns
CDATA Set Up Time	tcsu		450	850	ns
CDATA Hold Time	tchd		450	950	ns

3.3 Signal Timings

Item	Symbol	Min.	Max.	Unit
C/D Set Up Time	t_{CDS}	100	-	ns
C/D Hold Time	t_{CDH}	10	-	ns
CE, RD, WR Pulse Width	t_{CP}, t_{RP}, t_{WP}	80	-	ns
Data Set Up Time	t_{DS}	80	-	ns
Data Hold Time	t_{DH}	40	-	ns
Access Time	t_{ACC}	-	150	ns
Output Hold Time	t_{OH}	10	50	ns

Conditions: VCC=5±0.25V, GND=0V, Ta=25°C

Bus Timing



3.4 Memory Address and Display Position

[6 x 8 Font]

* Relationship between display memory address and display position on LCD module. In case of 6 x 8 Font, is defined in this section 3.4.1.

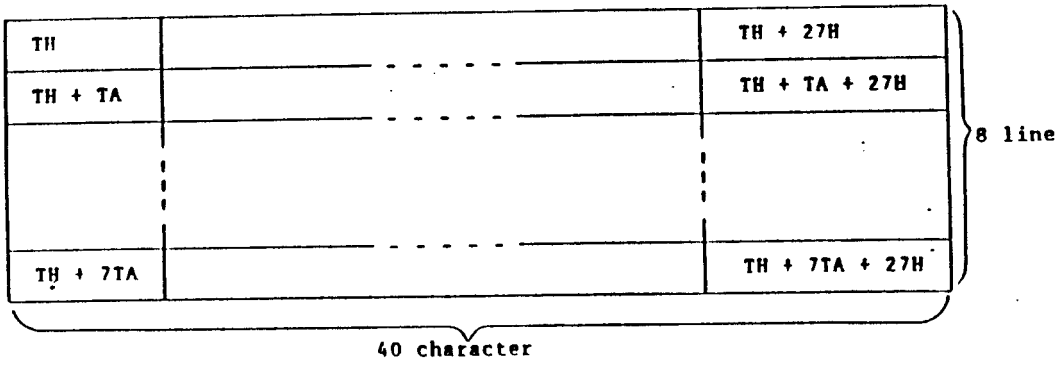
Graphic home address GH, number of graphic area GA, text home address TH, and number of text area TA are defined by "Control Word Set" command. The position of GH, TH is described in 3.4.3 RAM map.

3.4.1 Memory Address and Display Position

Text Display (Ex. 240 x 64 DOT)

TA = 28H, GA = 28H

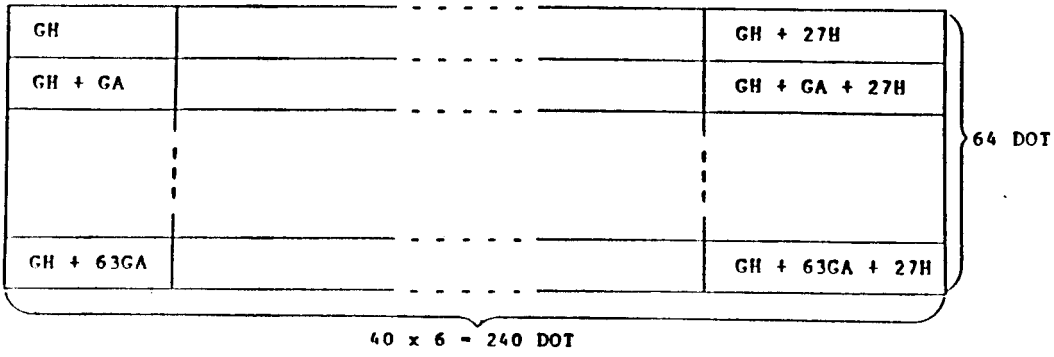
TH & GH = Within 0000H - 1FFFH



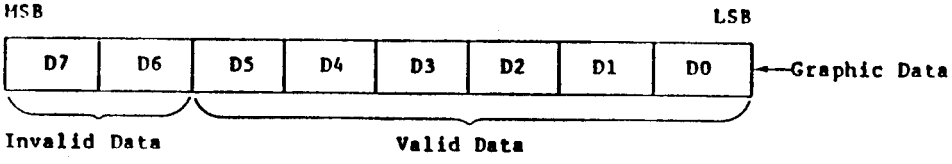
Graphic Display (Ex. 240 x 64 DOT)

TA = 28H, GA = 28H

TH & GH = Within 0000H - 1FFFH



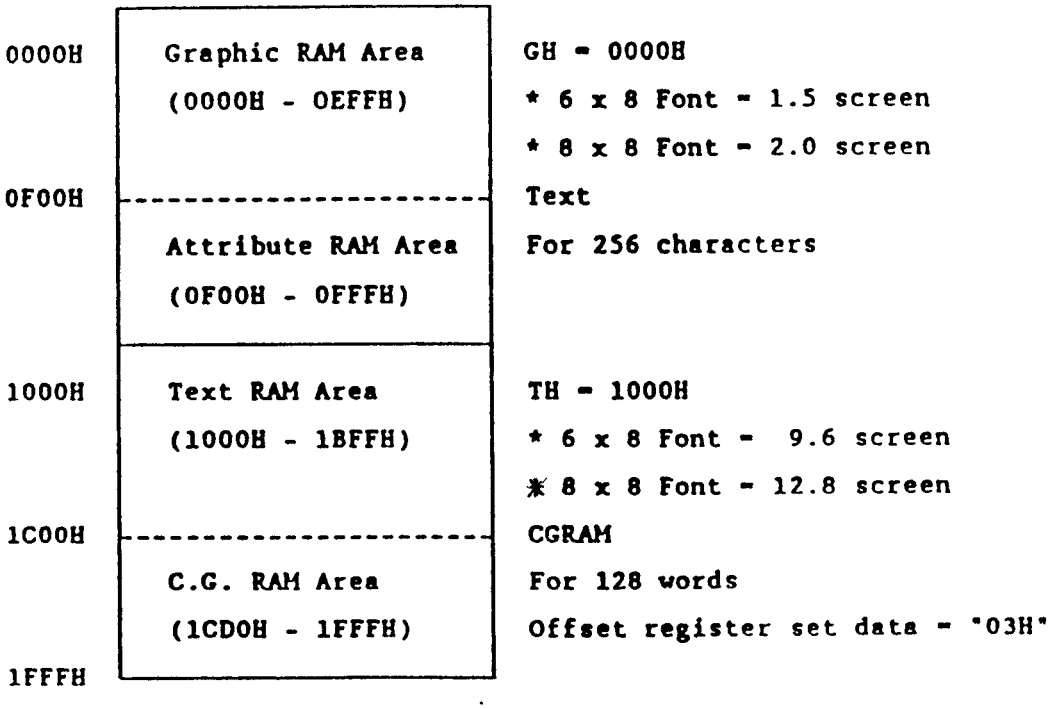
Note: In case of graphic display, 8 bit data is as follows:



3.4.3 RAM Map

Display RAM is built-in the module, and display data is written to this display RAM. Built-in controller LSI76963C is automatically read from display RAM, and send data to LCD drivers. "Control Word Set" command (text home set, text area set, etc.) defines the RAM area which is read by controller LSI, so RAM map can be changed by user's preference. If more than 1 screen can be stored in the RAM. Vertical scrolling and paging is easily performed by resetting text home and/or graphic home address.

EA 7000-K series have 8K byte built-in RAM located at address 0000H - 1FFFH, and the following is an example of RAM mapping (240 x 64 DOT).



4. Soldering Jumper Setting

4.1 Initial Setting

Initial setting for "Font" and "Column" are described in Table 4.1.

	Dot	Duty	Bias	Font	Column
EA 7160-7K	160 x 128	1/128	1/12	8 x 8	32 (valid 20)
EA 7128-6,8K	128 x 112	1/112	1/12	8 x 8	32 (valid 16)
EA 7160-7KC	160 x 128	1/128	1/12	8 x 8	32 (valid 20)
EA 7240-6K2	240 x 64	1/64	1/9	6 x 8 (FS-H)	64 (valid 40)
EA 7240-6K2EW	240 x 64	1/64	1/9	6 x 8 (FS-H)	64 (valid 40)

Table 4.1

4.2 Explanation of Each Soldering Jumper

EA 7160-7K & 7128-6,8K Series

	Column			
	32	40	64	80
J6	H	L	H	L
J7	H	H	L	L

Initial set: J6, J7 = H

EA 7240-6K2 Series

	Column			
	32	40	64	80
J2	H	L	H	L
J3	H	H	L	L

Initial set: J2 = H, J3 = L

	Character Font			
	5x8	6x8	7x8	8x8
J8	H	L	H	L
J9	H	H	L	L

Initial set: J8, J9 = L

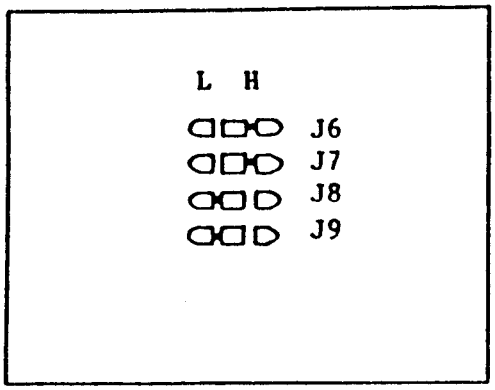
	Character Font			
	5x8	6x8	7x8	8x8
J4	H	L	H	L
FS	H	H	L	L

Initial set: J4 = L,
FS = Pull up (H)

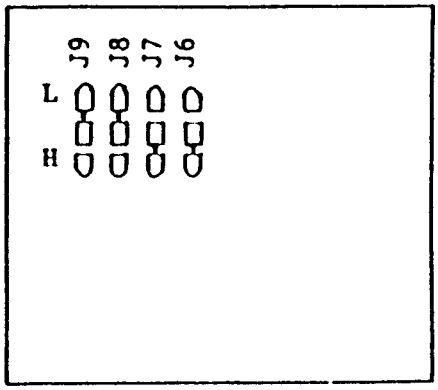
Note: H : +5V (Vec)
L : 0V (VSS)
FS: I/O terminal pin no. 19 for designate the "Font" from outside of the module.

* Jumper Position (FIX FROM FACTORY)

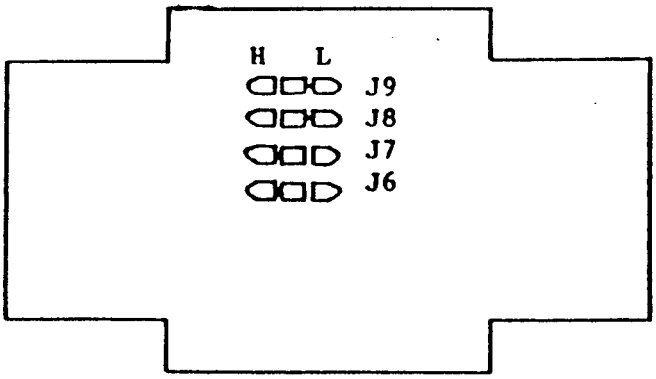
EA 7160-7K



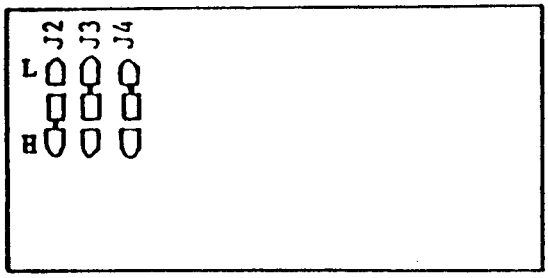
EA 7128-6,8K



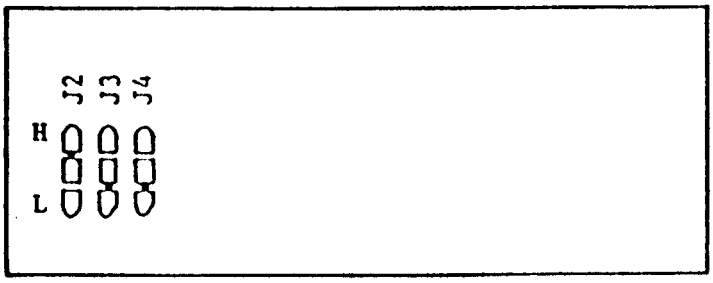
EA 7160-7KC



EA 7240-6K2



EA 7240-6K2C



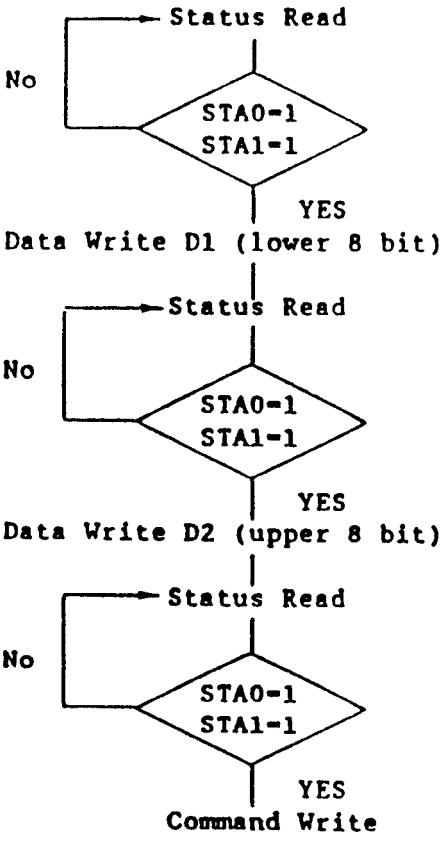
Note: All drawings are bottom view.

5. Communication between CPU and Module

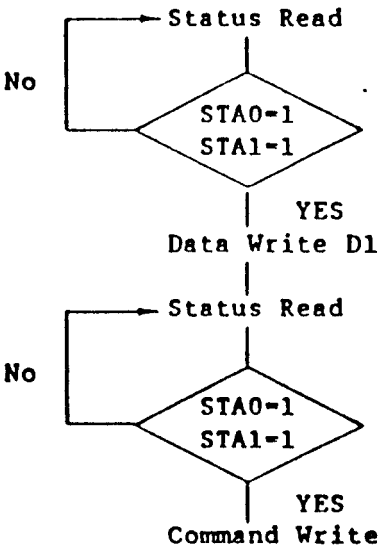
5.1 Data Transmission Method

Built-in LCD controller T6963C is operating asynchronously to CPU clock, and following procedure is required for data transmission between module and CPU.

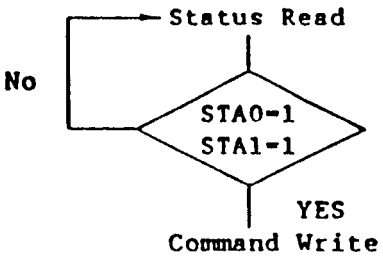
(1) Command with 2 byte data



(2) Command with 1 byte data



(3) Command with no data



(4) Data Auto Write/Data Auto Read

STA2, STA3 should be checked between all data and command.
(Refer 5.2.2.6 "Data Auto Write/Data Auto Read")

(5) Screen Peeking, Screen Copy

STA6 should be checked just after "Screen Peeking"/"Screen Copy".
(Refer 5.2.2.8/9 "Screen Peeking", "Screen Copy")

5.1.1 Status Read

Status of controller LSI shold be checked between all command and data in order to complete communication with CPU. Status can be read form 8 bit data lines (D0 to D7) by setting C/D="H", RD="L".

STA0 (Busy1)	Check capability of instruction execution	STA0=0 : Disable =1 : Enable
STA1 (Busy2)	Check capability of data read or data write	STA1=0 : Disable =1 : Enable
STA2 (DAV)	Check capability of data read (only effective in auto mode)	STA2=0 : Disable =1 : Enable
STA3 (RDY)	Check capability of data write (only effective in auto mode)	STA3=0 : Disable =1 : Enable
STA4	-	-
STA5 (CLR)	Check possibility of controller operation	STA5=0 : Disable =1 : Enable
STA6 (Error)	Address pointer is out of graphic area on screen peeking and screen copy command.	STA6=1 : Out of graphic area
STA7 (Blink)	Check the condition of blink	STA7=0 : Display off =1 : Normal display (on)

(Status Register)

STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0

MSB LSB

5.2 Command

5.2.1 Command List

Command	Command Code								Description	Execution Time (MAX) (Note 1)
	D7	D6	D5	D4	D3	D2	D1	D0		
Pointer Set	0	0	1	0	0	N2	N1	N0	N2 N1 N0 0 0 1 Cursor pointer set 0 1 0 Offset register set 1 0 0 Address pointer set	Status Check
Control Word Set	0	1	0	0	0	0	N1	N0	N1 N0 0 0 Text home address set 0 1 Text area set 1 0 Graphic home address set 1 1 Graphic area set	Status Check
Mode Set	1	0	0	0	CG	N2	N1	N0	CG-0: CG ROM Mode CG-1: CG RAM Mode N2 N1 N0 (Graphic and Text) 0 0 0 "OR" 0 0 1 "EXOR" 0 1 1 "AND" 1 0 0 Text only (attribute capability)	32x1/fOSC
Display Mode	1	0	0	1	N3	N2	N1	N0	N3-0: Graphic display off 1: Graphic display on N2-0: Text display off 1: Text display on N1-0: Cursor display off 1: Cursor display on N0-0: Cursor blink off 1: Cursor blink on	32x1/fOSC
Cursor Pattern Select	1	0	1	0	0	N2	N1	N0	N2, N1, N0 specify the number of cursor lines (EX) N2 N1 N0 0 0 0 1 line cursor (bottom line) 1 1 1 8 line cursor (8x8 dot cursor)	32x1/fOSC

Command	Command Code								Description	Execution Time (MAX) (Note 1)
	D7	D6	D5	D4	D3	D2	D1	D0		
Data Auto Read/Write	1	0	1	1	0	0	N1	N0	N1 N0 0 0 Data auto write set 0 1 Data auto read set 1 * Auto reset After this command, continuous data can be written or read. (address pointer automatically increment)	32x1/fOSC
Data Read/ Write	1	1	0	0	0	N2	N1	N0	Data read/write command for 1 byte. N2-0: Address pointer up/down -1: Address pointer unchanged N1-0: Address pointer up -1: Address pointer down N0-0: Data write -1: Data read	32x1/fOSC
Screen Peeking	1	1	1	0	0	0	0	0	Transfer display data to data stack for read from CPU.	Status Check
Screen Copy	1	1	1	0	1	0	0	0	1 line displayed data which address is indicated by address pointer is copied to graphic RAM area.	Status Check
Bit Set/ Reset	1	1	1	1	N3	N2	N1	N0	Set/reset command for a bit in the address pointer. N3-0: Bit reset -1: Bit set N2, N1, N0 indicate the bit in the pointed address. (000 is LSB, and 111 is MSB.)	Status Check

Note 1: Status check between all commands and data is recommended, though execution time for several commands are specified in above command list.
For the commands with "status check" in execution time, execution time does not specify because it is influenced by internal situation of controller LSI.

Note 2: In case of 2 screen mode, Screen copy command cannot be used.

5.2.2 Description of Command

5.2.2.1 Pointer Set Command

D1, D2,	0	0	1	0	0	N2	N1	N0

Command is selected by setting "1" at selected bit.

N2	N1	N0	Command	D1	D2
0	0	1	Cursor pointer set	Column position	Row position
0	1	0	Offset register set	Address	00H
1	0	0	Address pointer set	Address (Lower)	Address (upper)

(a) Cursor Pointer Set

The cursor is displayed at the position specified by the D1, D2. The cursor position is shift only by this command, and does not shift by other command like a "data write" command. D1, D2 are specified as follows.

D1 : Horizontal cursor position counted by "character" (5 - 8 dot width/character specified by hard setting.. refer 4 "Soldering Jumper Setting"). MSB of D1 is neglected, and 127 is the maximum.

D2 : Vertical cursor position counted by "character (8 dot high character) (1st row of lower half screen is "11H")
Upper 3 bit are neglected and 32 is the maximum.

Note: Please note that the cursor position should be within actual display area.

(b) Offset Register Set

Offset register set command is used to determined character generator RAM area. The upper 5 bits in start address of CG area is set as the lower 5 bits of D1, and upper 3 bits of D1 is neglected. D2 should be 00H. Refer 5.4 "Character Generator" for detail of CG RAM.

(c) Address Pointer Set

Address pointer set command is used to indicate the start address for writing data to built-in RAM, or for reading data from built-in RAM. The address should be located in the actual RAM area specified by individual specifications. (Refer to 3.4.3 "RAM MAP".)

5.2.2.2 Control Word Set Command

D1, D2,	0	1	0	0	0	0	N1	N0

Home address of display RAM (Text, Graphic), and areas are defined by this command.

N1	N0	Command	D1	D2
0	0	Text home address set (TH)	Address (lower)	Address (upper)
0	1	Text area set (TA)	No. of column	00H
1	0	Graphic home address set (GH)	Address (lower)	Address (upper)
1	1	Graphic area set (GA)	No. of column	00H

(a) Text Home Address Set (TH)

This command defines the starting address of display RAM for text display. The data in the text home address (TH) is displayed at the home position of display (left end character on 1st row).

(b) Text Area Set (TA)

This command defines the number of column by D1. Text area can be defined independent from character No. fixed by hard setting of controller LSI. Text area is usually defined the same number as the actual character number of LCD display, so address can be continuous in text area in this case.

(c) Graphic Home Address Set (GH)

This command defines the starting address of display RAM for graphic display. The data in the Graphic home address (GH) is displayed at the home position of display (left end 8 bits in 1st line). When using attribute function, Graphic home address indicates the starting address of distribute RAM area.

(d) Graphic Area Set (GA)

This command defines the number of column by D1. Graphic area can be defined independent from character No. fixed by hard setting of controller LSI. So address in graphic area can be continuous and RAM area can be used without uneffective area, if graphic area is defined the same number as the actual column number of LCD display. Note that Graphic area will be different by character font setting even if horizontal dot number is the same.

5.2.2.3 Mode Set Command

(No data)	1	0	0	0	CG	N2	N1	N0

Mode set command selects character generator (CG ROM Mode/CG RAM Mode), and combination of text/graphic display.

CG	Command
0	CG ROM Mode: Built-in 128 character CG ROM (code: 00H - 7FH) and built-in CG RAM for 128 characters can be used.
1	CG RAM Mode: Built-in CG RAM for 256 characters (code: 00H - FFH) can be used.

When CG ROM Mode is selected, character code 00H - 7FH is selected from built-in CG ROM and 80H - FFH is automatically selected from CG RAM.

N2	N1	N0	Command
0	0	0	Logically "OR" of Graphic and Text display
0	0	1	Logically "EXOR" of Graphic and Text display
0	1	1	Logically "AND" of Graphic and Text display
1	0	0	Text display only (text can be attributed by the data in graphic area)

Logically "OR", "EXOR" and "AND" of graphic and text display can be displayed by this command. Only text display is attributed because Attribute RAM is located in Graphic RAM area. (Refer 5.5 "Attribute")

5.2.2.4 Display Mode Set Command

(No data)	1	0	0	1	N3	N2	N1	N0

Display mode is selected from combination of following 4 bits by setting "1" at the selected bit.

	Command
N0	Cursor blink ON (N0=1)/Cursor blink OFF (No=0)
N1	Cursor display ON (N1=1)/Cursor display OFF (N1=0)
N2	Text display ON (N2=1)/Text display OFF (N2=0)
N3	Graphic display ON (N3=1)/Graphic display OFF (N3=0)

After hard reset, all displays are inhibited. (N0=N1=N2=N3=0)

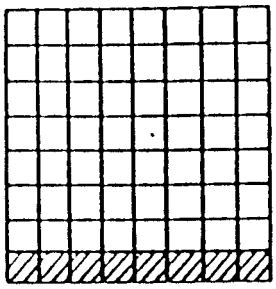
5.2.2.5 Cursor Pattern Select Command

(No data)	1	0	1	0	0	N2	N1	N0

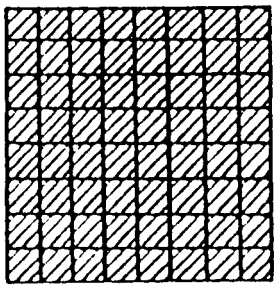
When cursor display is "ON", this command selects the cursor pattern from 1 line width cursor to 8 line width cursor (block).

N2	N1	N0	Cursor pattern
0	0	0	1 line width cursor
0	0	1	2 line width cursor
0	1	0	3 line width cursor
0	1	1	4 line width cursor
1	0	0	5 line width cursor
1	0	1	6 line width cursor
1	1	0	7 line width cursor
1	1	1	8 line width cursor

(1 line width cursor)



(8 line width cursor)



5.2.2.6 Data Auto Write/Data Auto Read

(No data)	1	0	1	1	0	0	N1	N0

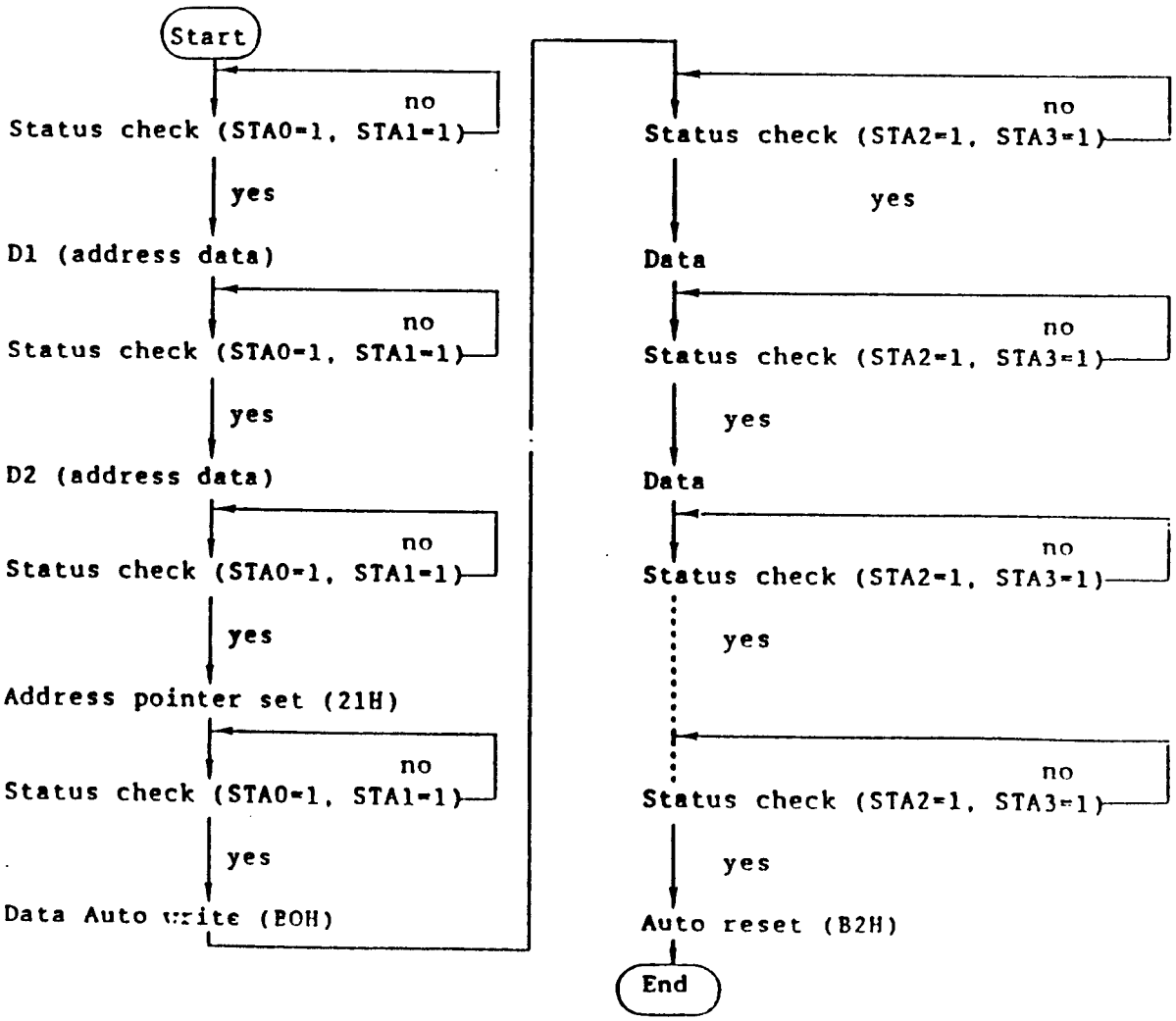
This command is convenient to send full screen data, or receive full screen data from built-in RAM. After setting auto mode, "data write (or read)" command is not necessary between each data. "Data auto write (or read)" command should follow the "address pointer set" and address pointer is automatically increment by +1 after each data. After sending (or receiving)

all data, auto mode reset is necessary to return normal operation because all data is regarded "display data" and no command can be accepted in the auto mode.

N1	N0	Command
0	0	Data Auto Write set
0	1	Data auto Read set
1	*	Auto Mode Reset

*: Don't care.

Note: Status check for auto mode (STA2, STA3) should be checked between each data. Auto reset should be performed after checking STA3=1 (Data Auto write only). Refer following chart.



5.2.2.7 Data Write/Data Read

D1,	1	1	0	0	0	N2	N1	N0

Note: D1 is necessary only for data write.

This command is used for data write from CPU to built-in RAM, and data read from built-in RAM to CPU. Data write/data read should be executed after setting address by address pointer set command.
Address pointer can be automatically increment or decrement by setting this command.

N2	N1	N0	
0	0	0	Data Write (after execution address pointer increment)
0	0	1	Data Read (after execution address pointer increment)
0	1	0	Data Write (after execution address pointer decrement)
0	1	1	Data Read (after execution address pointer decrement)
1	*	0	Data Write (after execution address pointer unchanged)
1	*	1	Data Read (after execution address pointer unchanged)

*: Don't care.

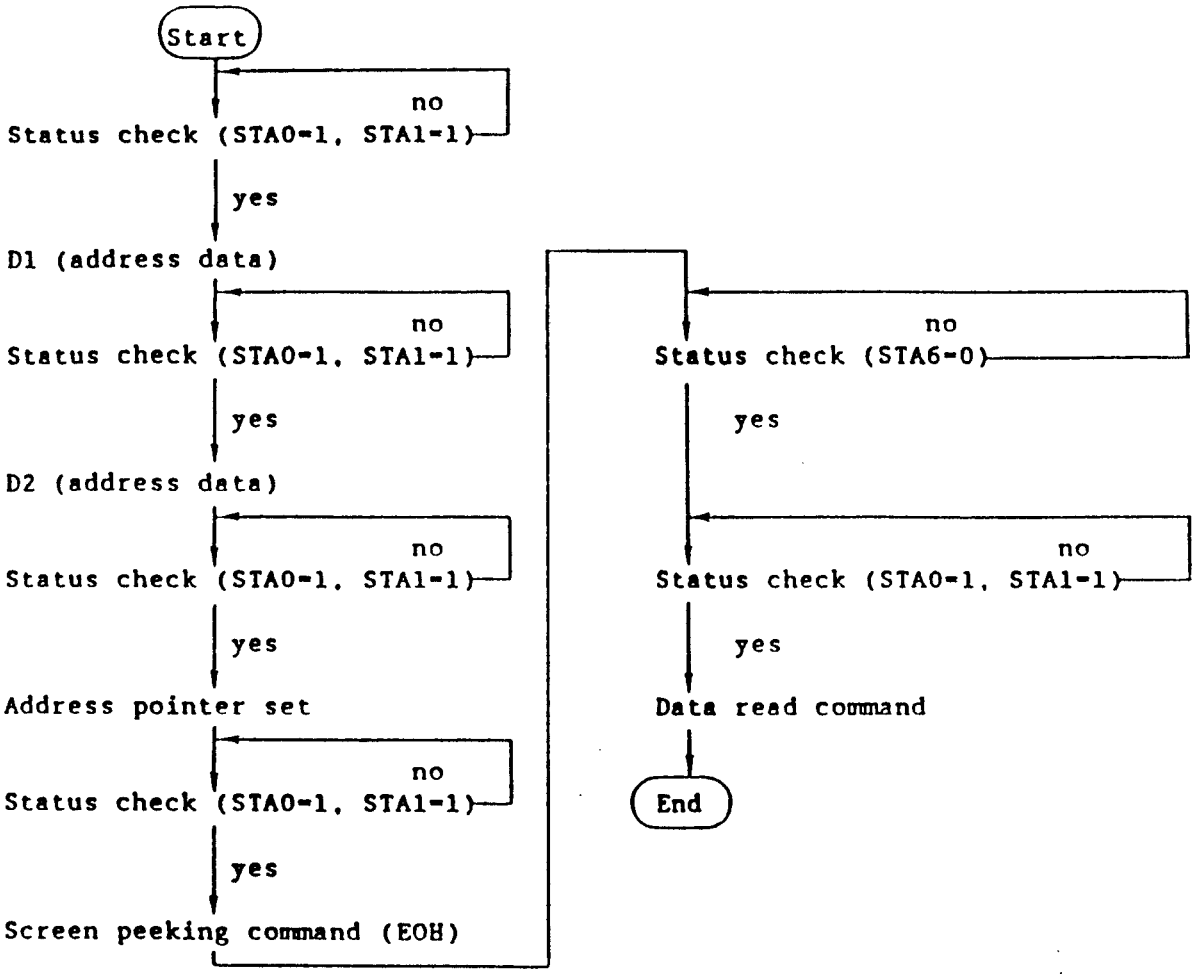
This command is necessary for each 1 byte data.

5.2.2.8 Screen Peeking

(No data)	1	1	1	0	0	0	0	0

This command is used to transfer displayed 1 byte data to data stack, and this 1 byte data can be read from CPU by data read command. So, logical combination data of text and graphic display on LCD screen can be read by this command. Status (STA6) should be checked just after "screen peeking" command. If the address determined by "address pointer set" command is not in graphic RAM area, this command is ignored and status flag (STA6) is set.

The procedure to read displayed data using this command is as follows.



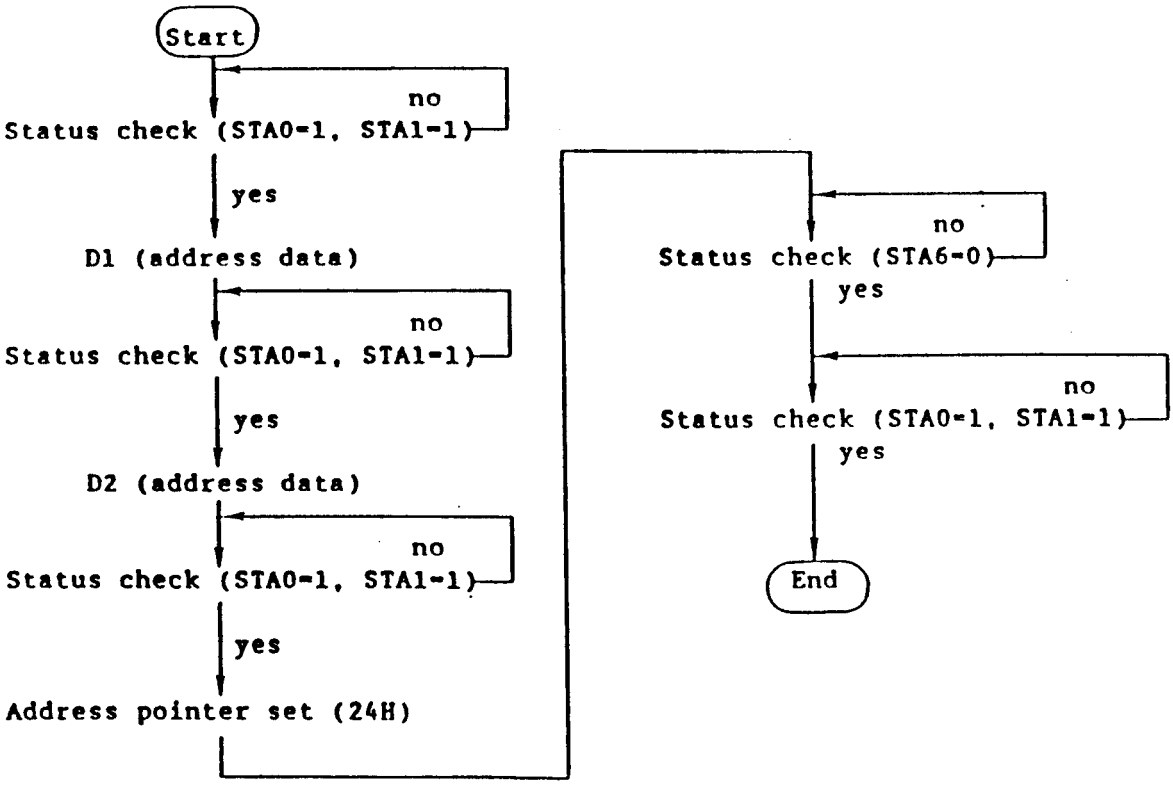
Screen peeking command can be used for getting hardcopy of LCD display. Another application of this command is that modified CG is set in the CG RAM area by reading combination data of text and graphic data and writing to CG RAM area. For example, CG for reverse character is made by this method.

5.2.2.9 Screen Copy

(No data)	1	1	1	0	1	0	0	0

1 low data displayed in LCD screen can be copied to the graphic RAM area specified by "address pointer set" command. Start point of 1 low data in the screen is determined by the "address pointer set" command. If attribute for text display is set by "Mode Set" command, "screen copy" command can not be used.

Status (STA6) should be checked just after this command. If the address determined by "address pointer set" command is not located in graphic RAM area, this command is ignored and status flag (STA6) is set. The procedure to copy the displayed data using this command is as follows.



Note: In case of 2 screen mode, Screen copy command cannot be used.

5.2.2.10 Bit Set, Bit Reset

(No data)	1	1	1	1	N3	N2	N1	N0

One bit in the 1 byte data specified by "address pointer set" command can be set or reset. Plural bits in the 1 byte data cannot be set/reset at a time.

	Description
N3	N3 = 1 : bit set, N3 = 0 : bit reset
N2 N1 N0	N2, N1, N0 specify the bit for set/reset. N2, N1, N0 0 0 0 bit 0 (LSB) 0 0 1 bit 1 0 1 0 bit 2 ⋮ ⋮ ⋮ 1 1 1 bit 7 (MSB)

5.3 Initialize

Initialize of controller LSI T6963C is required for "Mode set", "Control word set" after power on. Following is the one example of initialize procedure of 240 x 64 dot display.

Command	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Note
Power on	Power on									
Hard reset (Use reset terminal)	RESET="L" (1mSec minimum after VDD ≥ 4.75V)									
Mode set	1	1	0	0	0	0	0	0	0	"OR" mode
Control word set Graphic home position set (Graphic home position 0000H)	0 0 1	0 0 0	0 0 1	0 0 0	0 0 0	0 0 0	0 0 0	0 0 1	0 0 0	Graphic home address Command
Number of graphic area set (Graphic 30 x 8 dots)	0 0 1	0 0 0	0 0 1	0 0 0	1 0 0	0 0 0	1 0 0	1 0 1	1 0 1	Number of area command
Text home position set (Text home position 1000H)	0 0 1	0 0 0	0 0 1	0 0 0	0 1 0	0 0 0	0 0 0	0 0 0	0 0 0	Text home address Command

Command	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Note
Number of text area set (Text 30 column)	0	0	0	0	1	0	1	1	1	Number of area Command
	0	0	0	0	0	0	0	0	0	
	1	0	1	0	0	0	0	0	1	
(Initialize end) (Data write)										
Address pointer set (Address pointer 0000H)	0	0	0	0	0	0	0	0	0	Graphic home address Command
	0	0	0	0	0	0	0	0	0	
	1	0	0	1	0	0	1	0	0	
Data write (Graphic)	0	0	1	0	1	0	1	0	1	Data Command
	1	1	1	1	0	0	0	0	0	
	0	1	0	1	0	1	0	1	0	Data Command
	1	1	1	1	0	0	0	0	0	
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
Address pointer set (Address pointer 1000H)	0	0	0	0	0	0	0	0	0	Text home address Command
	0	0	0	0	1	0	0	0	0	
	1	0	0	1	0	0	1	0	0	
Data write (Text) (o)	0	0	0	1	0	1	1	1	1	Data command
	1	1	1	0	0	0	0	0	0	
(p)	0	0	0	1	1	0	0	0	0	Data command
	1	1	1	0	0	0	0	0	0	
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
Display Mode Set (Text/Graphic on)	1	1	0	0	1	1	1	0	0	

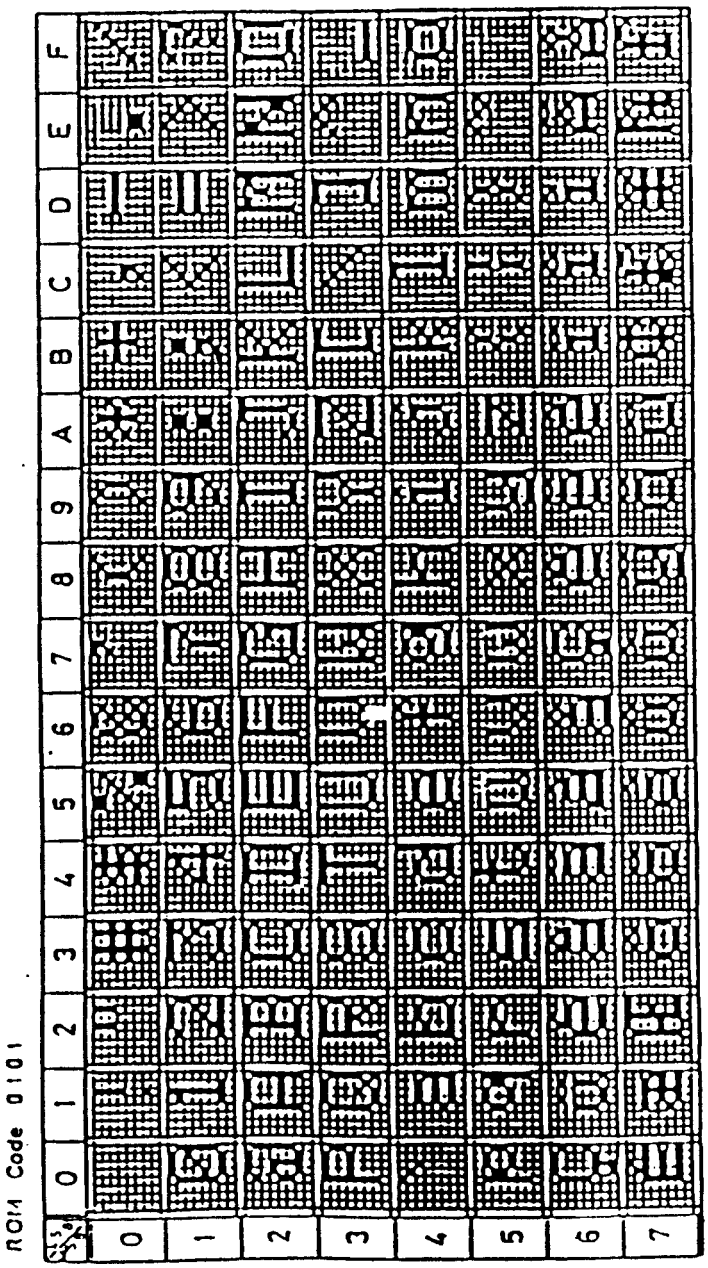
Note 1: "Status check" should be inserted between all command and data.
2: Display mode set register is cleared (no display mode) by the hard reset, and no display is appeared on LCD panel. And just after "Display Mode set 9CH", written data is displayed on the LCD.

5.4 Character Generator

5.4.1 Character Generator ROM

Character generator ROM for 128 characters is built-in this module.

Character code map



5.4.2 User Character Generator RAM

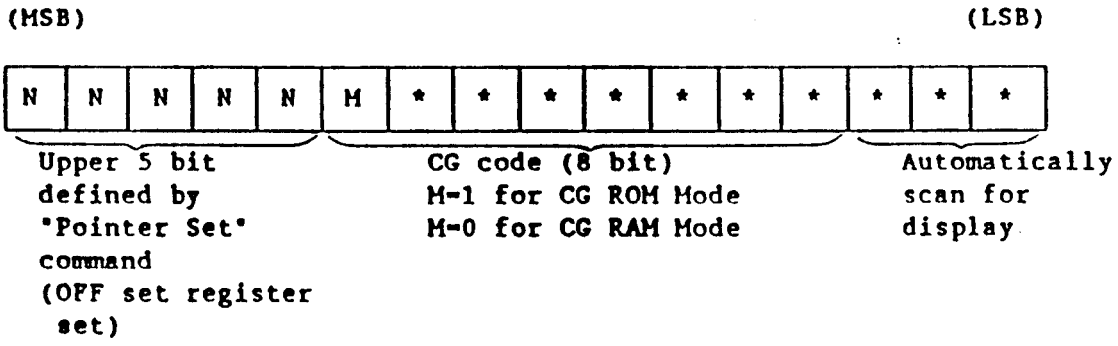
Character generator RAM is the built-in RAM which can be used as character generator after writing character pattern by progRAM. The part of built-in RAM can be used as "User CG RAM" for 256 characters by selecting "CG RAM Mode", or for 128 characters by selecting "CG ROM Mode".

(1) Position of User CG RAM

The upper 5 bits in start address of User CG RAM (NNNNN) is defined by "Pointer Set" command (Offset register set), and following 2048 byte are defined as "User CG RAM" area when CG RAM Mode is selected. 1024 byte (address: NNNNN10000000000 NNNNN11111111111) is defined as "User CG RAM" are when CG ROM Mode is selected.

(2) Writing to User CG RAM

Character pattern of specified CG code can be written in the pointed address by "Pointer Set" command (Address pointer set). 8 byte data should be sent to following 8 byte address for 1 character.



(3) Display Pattern in User CG RAM

Character pattern can be displayed by sendined CG code with "Data Write" command. But "Display Mode Set" for text display should be selected before using CG. In case that "CG ROM Mode" in selected, character pattern is selected from built-in CG ROM when MSB=0 (00H-7FH), and from User CG RAM when MSB=1 (80H-FFH). In case that "CG RAM Mode" is selected, all character patterns are selected from User CG RAM (00H-FFH).

(4) Relation between User CG RAM Address and CG code and Character Pattern

When character pattern is written to User CG RAM, relation between CG code and "User CG RAM" address is shown in the following chart.

Character Code 7 6 5 4 3 2 1 0	RAM Address for User CG F E D C B A 9 8 7 6 5 4 3 2 1 0	Character Pattern 7 6 5 4 3 2 1 0
M 0 0 0 0 0 0 0	N N N N N M 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	0 0 1	0 0 0 0 1 0 0 0
	0 1 0	0 0 0 0 0 1 0 0
	0 1 1	0 1 1 1 1 1 1 0
	1 0 0	0 0 0 0 0 1 0 0
	1 0 1	0 0 0 0 1 0 0 0
	1 1 0	0 0 0 0 0 0 0 0
	1 1 1	0 0 0 0 0 0 0 0
M 0 0 0 0 0 0 1	N N N N N M 0 0 0 0 0 0 1 0 0 0	0 1 0 0 0 0 1 0
	0 0 1	0 1 1 0 0 1 1 0
	0 1 0	0 1 0 1 1 0 1 0
	0 1 1	0 1 0 1 1 0 1 0
	1 0 0	0 1 0 0 0 0 1 0
	1 0 1	0 1 0 0 0 0 1 0
	1 1 0	0 1 0 0 0 0 1 0
	1 1 1	0 0 0 0 0 0 0 0
M 0 0 0 0 0 1 0	N N N N N M 0 0 0 0 0 1 0 0 0 0	0 1 0 0 0 0 1 0
	0 0 1	0 1 1 0 0 0 1 0
	0 1 0	0 1 0 1 0 0 1 0
≈	≈	≈
	1 1 1	0 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1	N N N N N 1 1 1 1 1 1 1 1 1 0 0 0	0 1 1 1 0 0 0 0
	0 0 1	0 1 0 0 0 0 0 0
	0 1 0	0 1 1 1 1 0 1 0
	0 1 1	0 0 0 1 1 0 1 0
	1 0 0	0 1 1 1 1 0 1 0
	1 0 1	0 0 0 0 1 1 1 0
	1 1 0	0 0 0 0 1 0 1 0
	1 1 1	0 0 0 0 1 0 1 0

Note 1: Character code in "User CG RAM" is located from 80H to FFH in case of "CG ROM Mode", and from 00H to FFH in case of "CG RAM Mode". So, M in above chart is as follows.

M=1 : "CG ROM Mode"

M=0 : "CG RAM Mode"

Note 2: "NNNNN" is the upper 5 bits in start address of User CG RAM defined by "Pointer Set" command (Offset Register Set).

3: It must be careful so that User CG RAM area should not be rewritten by display data, etc.

5.5 Attribute

5.5.1 Attribute Function

This module has attribute function for "Reverse display", "Blink" in text display mode. Attribute data is written in the "Graphic area" defined by "Control word set" command (Graphic home address set and Graphic area set)'. So "Text display only" Mode should be selected by "Mode Set" command, and graphic display cannot be displayed.

The attribute data of the 1st character in "Text area" is written at the 1st 1 byte in "graphic area", and attribute data of nth character is written at the nth 1 byte in "Graphic area". Attribute function is defined as follows.

Attribute RAM

1 byte

*	*	*	*	N3	N2	N1	N0

N3	N2	N1	N0	Function
0	0	0	0	Normal display
0	1	0	1	Reverse display (Text only)
0	0	1	1	Inhibit display
1	0	0	0	Blink of normal display
1	1	0	1	Blink of reverse display
1	0	1	1	Inhibit display

* : Don't care.

5.5.2 Procedure of setting attribute

The example of the procedure of setting attribute is as follows.

Command	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Note
Graphic display off	1	1	0	0	0	0	*	*	*	
Graphic home address set	0	0	0	0	0	0	0	0	0	home address 1400H command
	0	0	0	0	1	1	0	0	0	
	1	0	1	0	0	0	0	1	0	
Attribute data write	0	0	0	0	0	0	0	0	0	address 1400H address pointer attribute data write command attribute data write command
	0	0	0	0	1	1	0	0	0	
	1	0	0	1	0	0	1	0	0	
	0	0	0	0	0	0	0	0	0	
	1	1	1	0	0	0	0	0	0	
	0	0	0	0	0	1	1	0	0	
	1	1	1	0	0	0	0	0	0	
	.	.	.	.	.	.	.	.	.	
	.	.	.	.	.	.	.	.	.	
Mode set	1	1	0	0	0	0	1	0	0	
Graphic display on	1	1	0	0	0	1	*	*	*	

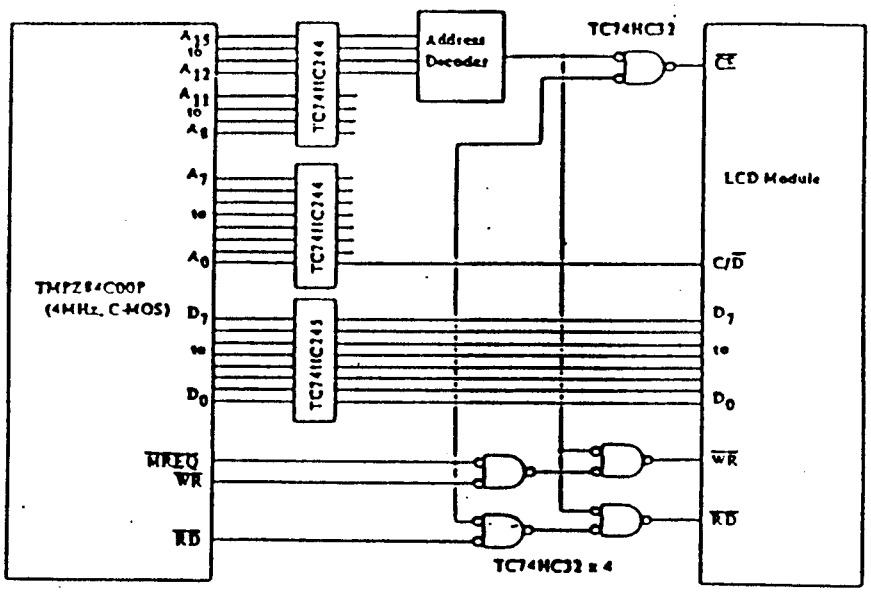
*: Don't care.

6. Application Circuits

Following diagRAMs are the examples of interface circuit with CPU TMPZ84C00P (Z80, CMOS 4MHz). For the interface to 16 bit CPU, please refer the diagRAM using PPI LSI (TMP82C55).

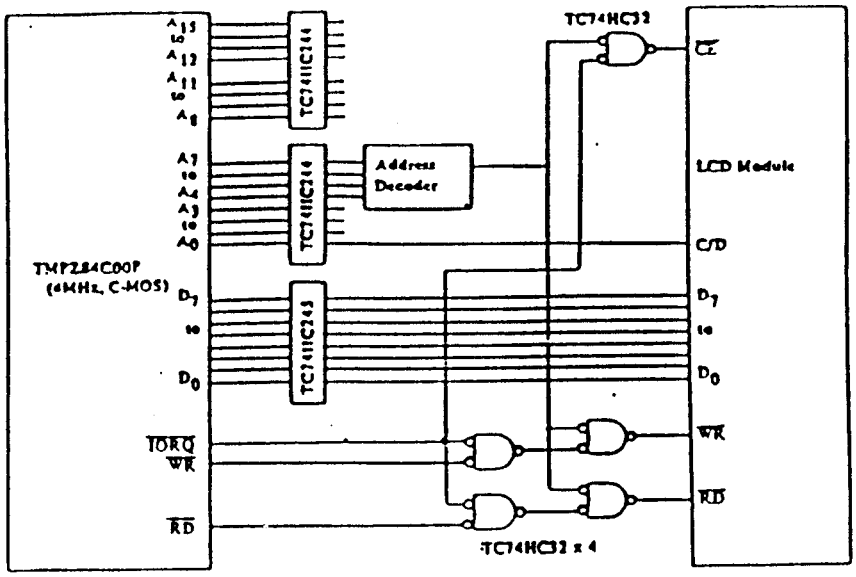
6.1 Module Located in the Memory Area of CPU

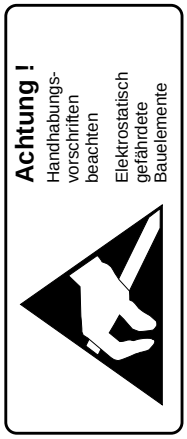
The module can be directly connected to CPU data bus as following diagRAM. Control signals of the module are made from MREQ, WR, RD signals of CPU, and chip select signal from address decoder. LSB of address bus (A0) can be used as C/D (command/data selection) signal.



6.2 Module Located in the I/O Area of CPU

The module can be controlled as the device located in the I/O area. Control signals are made from IORQ, WR, RD of CPU, and the chip select signal from address decoder. LSB of address bus (A0) can be used as C/D (command/data selection) signal.





6.3 Interface Circuit with PPI LSI (TMP82C55)

The module can be interfaced with PPI LSI as shown following diagRAM. 8 bit data bus of the module is connected to A port of PPI, and control signals (C/D, CE, WR, RD) are sent from upper 4 bit of C port. In following diagRAM PPI is located in the I/O address area, but interface between CPU and PPI can be left for user's design.